Accumulated body ultranarrow channel silicon transistor with extreme threshold voltage tunability

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(Received 21 May 2007; accepted 7 November 2007; published online 10 December 2007)

A side-gated ultranarrow channel (width <10 nm) silicon field effect transistor (FET) with extreme threshold voltage (V_t) tunability is described. A narrow inversion layer is formed on the top interface controlled by the top gate. The device body and side interfaces are accumulated by up to 10^{19} cm^{-3} holes, drawn from the substrate by negatively biased side gates (V_{side}), increasing V_t by 3 V, suppressing peripheral leakage currents and short channel effects. V_t response to V_{side} follows a square root behavior, $dV_t/d\sqrt{-V_{side}}=3.73\ \mathrm{V}/\sqrt{\mathrm{V}}$, similar to that of body doping. Maximum linear tunability (dV_t/dV_{side}) exceeds -2 V/V, average dV_t/dV_{side} is -1.67 V/V. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2818663]

Multigate structures, such as double-gate, back-gate, fin-shaped field-effect transistor (FinFET), etc., have been investigated as approaches to control power in tens of nanometer of scale due to good short channel control and threshold voltage tuning through a second gate.[1,2] Multigate FETs also combine the flexibility of electrostatic tuning of V_t of individual devices with control of leakage pathways at very short gate lengths (L_g). An additional gate also opens possibilities of alternative circuit approaches where higher versatility and functionality is achieved at lower power. Lower power[3] and lower voltages in such structures require strong threshold tuning and lower dimensions require increased immunity to stochastic effects, such as those arising from dopants and interface defects.

Earlier reports on high sensitivity V_t-tunable devices predominantly refer to double-gate structures that harness the electrostatic potential change caused from a back gate on the front channel of the transistor, with the two gates parallel to each other straddling a thin layer of Si channel.[1] Here, we provide for tuning gates on the two sides of an ultranarrow fin ($W_{si}<10$ nm), perpendicular to the main gate (Fig. 1).[4] These tuning side gates are utilized to draw holes from the substrate, reducing depletion depth substantially through accumulation, resulting in extreme electrostatic V_t control with a sensitivity far exceeding reports so far.[2] The central feature of this structure is its ability to provide large fields over short distances through the use of large induced carrier densities, and, thus, achieve extreme threshold voltage tuning.

Our devices are fabricated using *i*-line photolithography and standard complementary metal-oxide semiconductor (CMOS) processing techniques. The active areas of the devices are lithographically defined and etched using Cl_2/BCl_3 reactive ion etching (RIE) and SiO_2 hard mask. The body doping is increased by implantation of boron and diffusion of boron from the interfaces from a highly doped SiO_2 film. Highly doped SiO_2 is formed by depositing $p+$ (boron) doped polycrystalline silicon on the structures, followed by thermal oxidation in H_2O ambient that consumes all of the deposited polycrystalline silicon and a significant portion of the active area silicon from the sides. Boron, left in the SiO_2 formed on the surface, is diffused into the Si body through annealing. The SiO_2 is then etched in hydrofluoric acid (HF). Through this process, 0.25 μm wide active areas connecting the contact regions are thinned down to approximately 10 nm while achieving extremely smooth edges. A thin layer of Si_3N_4 is deposited followed by deposition of a thin layer of $n+$ (phosphorus) doped polycrystalline silicon film which

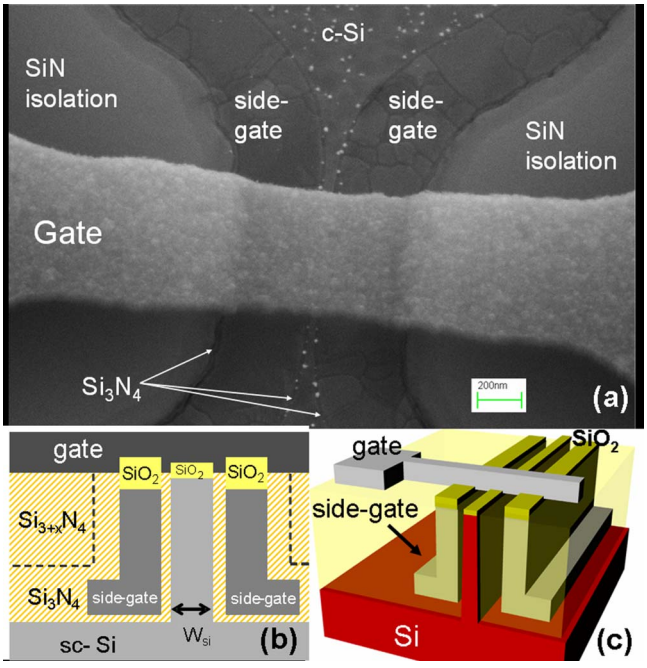

FIG. 1. (Color online) (a) Scanning electron microscopy image of a side-gated FET. The *in situ* doped polycrystalline silicon side gates are isolated from the single-crystal Si (sc-Si) active area by a thin layer of Si_3N_4. Thermally grown SiO_2 isolates the top gate from the active area and the side gates. (b) Cross-section schematics along the width of the device. Current flow is at the top Si–SiO_2 interface in and out of plane. STI is composed of Si_3N_4 and low stress silicon nitride. $t_{ox}\sim 4$ nm. (c) three-dimensional schematics of the device structure.

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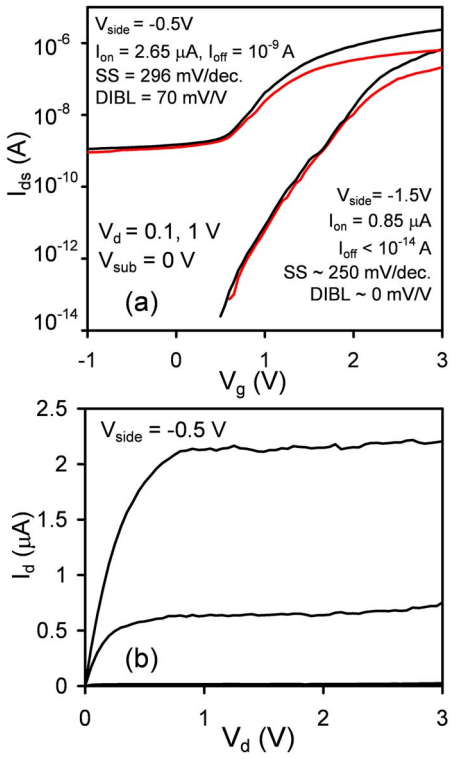

FIG. 2. (Color online) Electrical characteristics of an ultranarrow channel device. Estimated channel width is 7 nm. (a) Transfer characteristics for V_{side}=−0.5 and −1.5 V and V_d=0.1 V (red) and 1 V (black). Subthreshold behavior indicates charge trapping and detrapping events at the side silicon–silicon nitride interfaces. Drain induced barrier lowering (DIBL) is very small. (b) Output characteristics for V_{sub}=0 V and V_g=0–3 V and 1 V steps.

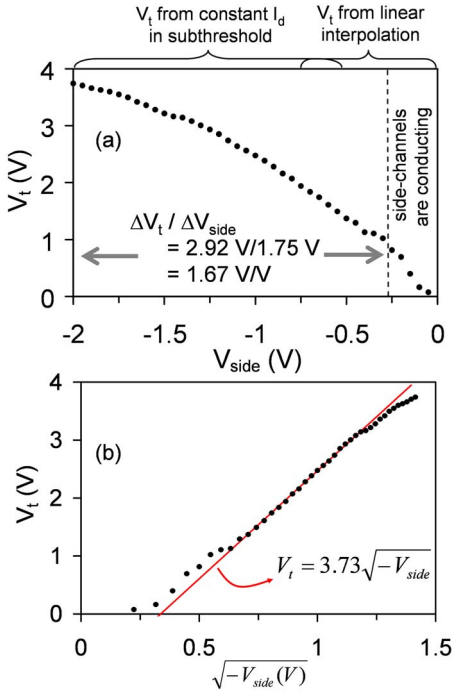

FIG. 3. (Color online) (a) Threshold voltage response to V_{side}, extracted using constant current method in subthreshold regime and linear interpolation in the "on" regime. (b) V_t graphed as a function of square root of $-V_{side}$.

will form the side gates. The polycrystalline silicon film is patterned around the active areas, with a lead extending to a contact area and etched by RIE. A thin layer of Si_3N_4 and a thicker layer of low stress silicon nitride are deposited as field isolation. The wafers are planarized using chemical mechanical polishing, exposing the active areas of the devices. A thin oxide is thermally grown on the exposed active area (gate oxide, t_{ox}=4 nm) and side gate surfaces in O_2/N_2 ambient followed by deposition of a thin layer of *n*+ doped polycrystalline silicon film, which will form the top gate. The polycrystalline silicon is lithographically patterned and etched using RIE. Thin oxide spacers are thermally grown and the wafers are implanted with arsenic and annealed to form self-aligned source/drain contacts. After depositing SiO_2 passivation and opening the vias, metal contacts are formed by Ti/Al lift-off. The samples are then annealed in H_2/Ar.[4–6]

The side gate surrounds the active area of the device like a guard ring and extends to a contact area under Si_3N_4 field isolation. The negative biasing of the side gate turns off the FETs formed on the two side interfaces (Fig. 1), suppressing the source to drain leakage current by more than a factor of 10^8 and significantly reducing the drain-to-substrate leakage.[4,7–10] Transistor operation is carried out by the independently controlled top gate (Fig. 2).[4–6]

The electrical results presented in this paper are from a device with estimated effective width (W_{eff}) of approximately 7 nm and gate length (L_g) of ~0.2 μm (Fig. 2), a good approximation to a nanowire FET. W_{eff} is estimated from the maximum transconductance (g_m~2.2 μA/V) observed for this device by referencing to the maximum transconductance of wider devices of known width with similar gate lengths (g_m/W_{eff}~0.35 μA/V/nm). This estimation assumes that the device's width is uniform along the channel and disregards possible variations in carrier mobilities as a function of device width. Gate oxide thickness is approximately 4 nm, as extracted from capacitance-voltage (*C-V*) measurements performed on larger devices on the same substrate. Gate oxide thickness of the presented device may be thicker due to oxygen diffusion from the top corners.

V_t sensitivity to V_{side} ($\delta V_t/\delta V_{side}$) exceeds −2 V/V in V_{side}=−1–−0.5 V region [Fig. 3(a)]. The dynamic range for the V_t is larger than 3 V with an average sensitivity of −1.55 V/V. V_t response to $\sqrt{-V_{side}}$ is linear with a slope of 3.73 $\sqrt{}$V in a wide range [Fig. 3(b)]. V_t does not respond to substrate bias (V_{sub}). No drain induced barrier lowering (DIBL) is evident for large negative side biases, however, DIBL and subthreshold slope (SS) degrade for increased negative V_{sub} for a constant V_{side}. V_t variation of ~0.1 V is observed in repeated measurements, which can be attributed to extreme sensitivity of this ultranarrow device to trapping and detrapping events on particularly the side interface where Si_3N_4 was employed. Positive fixed charges at the $Si-Si_3N_4$ side interfaces are expected to help suppress gate induced drain leakage at the side interfaces.

For a narrow channel device, accumulation at the side interfaces counters the depletion at the *p-n* junctions. This results in accumulation of the otherwise depleted volume under the channel and source/drain extensions (Fig. 4).[11] Larger negative V_{side} pulls holes beyond the source/drain metallurgical junctions, inverting the low doped edges of the source/drain extensions.

Accumulation of holes at high densities in this region results in a significant reduction in the depletion depth under the gate with high side-gate coupling. The accumulation con-

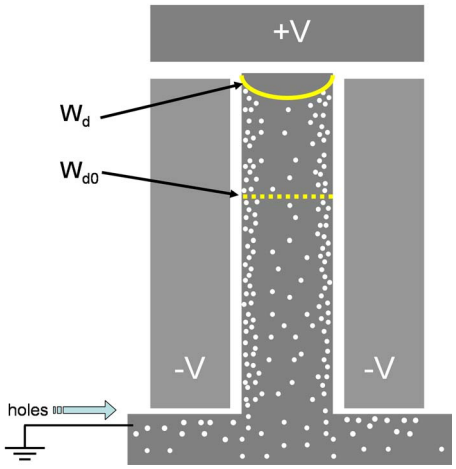

FIG. 4. (Color online) Cross-section schematic illustrating accumulated body operation. Holes are drawn from the substrate, connected to ground, into the device body. W_{d0} is the depletion depth under the top gate for a wide device. In the ultranarrow channel device W_{d0} is reduced to W_d due to accumulation of the body with holes when a large negative V_{side} is applied.

structs a large potential barrier between the source and the drain, suppresses DIBL, and punch-through.

The density of holes accumulated in the volume under the gate increases linearly with $-V_{side}$ reaching an approximate surface concentration of 4.5×10^{12} cm^{-2} at each side surface, corresponding to a volume concentration of 1.3×10^{19} cm^{-3} for a 7 nm width for $V_{side}=-2$ V. Depletion depth is expected to be approximately 10 nm for the given bias condition. The V_t at the top interface increases with the square root of the charge that the top gate has to counter (Fig. 3).[11] This V_t response is similar to that of body doping, hence, accumulation of the body can be thought of as electrostatic doping.

The hole accumulation has two important aspects. The first is that the accumulated hole density is large (10^{19} cm^{-3}), significantly larger than what can be achieved by doping. The second is that the device structure, in its nanowire limits, brings the holes right up to the inversion layer. The density of tuning charge is maximized and length scale for tuning is minimized. This is the most optimum control condition possible and does not exist in other approaches attempted to date.

The nonuniform distribution of holes under the channel is expected to result in a V_t variation along the width of the device leading to degradation of the subthreshold slope. This is more pronounced as device width is increased and dielectric thicknesses are reduced allowing larger variations in the electric field distribution (Fig. 4). Besides, increased coupling to the side gates and the body also degrades the subthreshold slope. Understanding the confinement effects and the parabolic potential profile formed along the width of the device requires rigorous computational evaluation of the case.

Accumulated body operation is, in many ways, similar to using halo implants for suppression of short channel effects, but with the additional advantage of electrostatic tuning and higher density.

In conclusion, an ultranarrow channel side-gated metal-oxide-semiconductor FET with accumulated body operation exhibiting significantly suppressed leakage currents and short channel effects is demonstrated, all using bulk silicon substrates. Control of threshold voltage and channel charge confinement via an immediately adjacent accumulation layer provides the structure with extreme threshold voltage tuning through side gates. Implementation of this structure with SiO_2 side dielectrics will reduce the variations in the device behavior due to charge trapping at the side interfaces. However, lack of fixed positive charges at the side interfaces is expected to reduce the onset of side gate induced band-to-band tunneling which may result in increased I_{min} levels. The side-gate dielectric thickness also needs to be adjusted to achieve the optimum sensitivity and subthreshold slope.

This approach allows tuning of individual devices for matching for analog applications, and has potential for alternative approaches for analog applications and for multi-input logic. It may also enable further scaling of CMOS devices by alleviating problems due to random dopant effects through use of intrinsic body[3] and electrostatic adjustment of the threshold voltages, while maintaining very low levels of leakage currents.

This work was supported in part by the National Science Foundation. Device fabrication was performed at Cornell NanoScale Science and Technology Facility.

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