Random telegraph signal in nanoscale back-side charge trapping memories

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Random telegraph signal (RTS) was observed in the front and back channel source-drain current of nanoscale double-gated back-side charge trapping memories. The front gate dielectric is silicon oxide and the back gate dielectric is a stack of silicon oxide–silicon nitride–silicon oxide (ONO). The structure provides a tool for traps characterization at multiple interfaces and combinations of materials. Bias dependence of RTS due to a trap in the back ONO was measured to determine the position of the trap in the dielectric. The results show that the individual trap is located within the tunneling oxide, 1.3 nm away from the silicon interface. RTS due to traps responsible for the memory properties, located in the silicon nitride or its interface, was not observed. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2182070]

Random telegraph signal (RTS) in small area transistors—discrete switching in the current between two or more levels under constant bias conditions—has been a favored tool in the study of individual traps in the silicon–silicon dioxide system.[1–3] RTS occurs due to charge trapping and detrapping events caused by individual traps near the $Si-SiO_2$ interface. The charge transfer event affects both the number and the mobility of the carriers in the channel resulting in a change in current that corresponds to carrier capture and emission by a single trap. From the bias dependence of the capture and emission times the location of the traps can be determined. An important question is how far deep into the gate dielectric can RTS reveal individual traps through its Coulombic interaction, and whether RTS can be used to study traps in devices where trapping is actively employed for achieving memory properties.[4,5] This work reports the study of room temperature RTS in nanoscale back-side charge trapping memory devices.

Back-side charge trapping memory devices are double gate structures in which the front gate dielectric is SiO_2 and the back gate dielectric is an oxide–nitride–oxide (ONO) film stack. Figure 1 shows a schematic cross section of a back-side trapping device and a transmission electron microscope (TEM) cross-section analysis of the back ONO stack between the single crystal silicon channel (intrinsic or lightly doped) and the single crystal silicon substrate (*n*-type heavily doped) that acts as the back gate. The silicon body is approximately 15 nm thick, the front oxide is 6 nm, and the back ONO stack is approximately 3, 4, and 7 nm, respectively. This substrate is prepared using a Smart-Cut[6] technique based on wafer bonding and hydrogen-induced exfoliation. The tunneling silicon oxide is thermally grown, the silicon nitride layer is deposited by low pressure chemical vapor deposition, and the control silicon oxide layer, where the bonding takes place, is the combination of deposited low temperature oxide and thermally grown oxide.

Charge stored in the large trap density region in the silicon nitride and its interface ($\sim 10^{12}-10^{13}$ cm^{-2})[7] is used to modify the threshold voltage of the device. By applying a large electric field between the back gate and the three front terminals, charge transport between the back-silicon channel and the nitride can occur by direct tunneling and Fowler–Nordheim tunneling. The decoupling of storage (back) from read/sense (front) allows superior scaling of the front oxide and eliminates charge injection damage to it. This distinguishes this structure from front-side charge trapping devices and allows it to be scaled to much smaller dimensions. The details on the fabrication and the memory characteristics of these small scale memory devices were previously published.[7,8]

We have observed RTS features in the front and back channel source-drain current of back-side charge trapping memories. Figure 2 shows the front channel output characteristics of a 50 nm × 50 nm ($W \times L$) back-side trapping device with RTS features. This RTS is due to a trap located in the front dielectric (oxide). Figures 3(a) and 3(b) show the front channel and back channel transfer characteristics of a 200 nm × 50 nm device, also exhibiting RTS features, in this case due to a trap located in the back dielectric (ONO). We can determine if a particular RTS signal corresponds to a trap in the front or back dielectric by its dependence on the front-

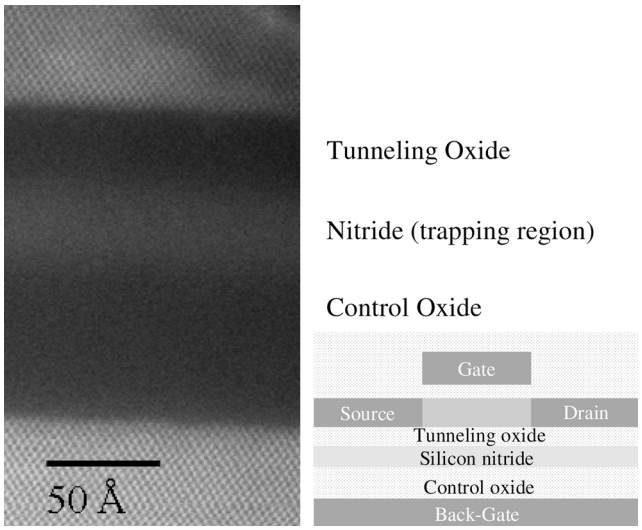

FIG. 1. Schematics of a back-side charge trapping memory device and TEM cross-sectional image of the back oxide–nitride–oxide (ONO) stack between the single crystal silicon substrate (back gate) and the single crystal silicon channel.

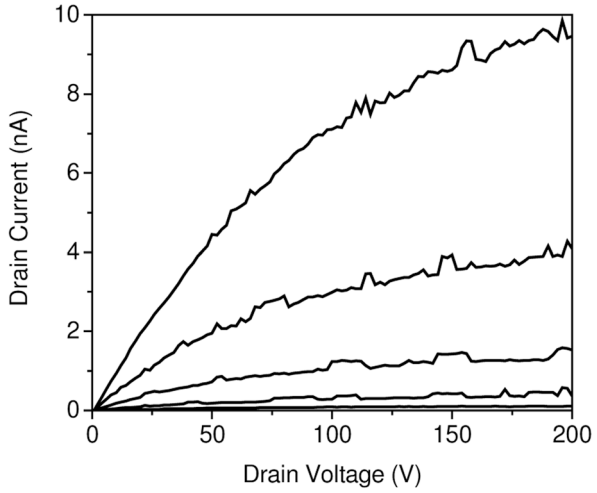

FIG. 2. Front channel output characteristics of a back-side charging device exhibiting RTS features: $W\times L=50\ \text{nm}\times 50\ \text{nm}$. $V_{\text{FG}}=0-0.4$ V, $V_{\text{BG}}=0$ V, $V_S=0$ V.

or back-gate bias: the average capture (emission) time decreases (increases) with the increase of the respective gate bias. Figures 3(a) and 3(b) also illustrate the double-gate operation of the device: inversion channels can be formed both on the front and the back silicon interfaces, and the threshold voltage in either of these modes can be modulated by the corresponding back bias.

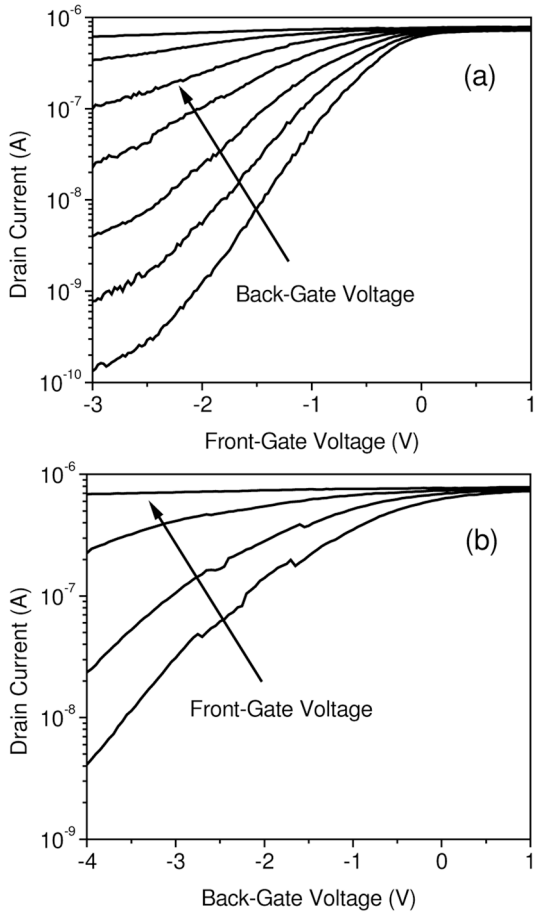

FIG. 3. Transfer characteristics of a back-side trapping memory device illustrating the double gate operation of the device and RTS features: $W\times L=200\ \text{nm}\times 50$ nm; (a) front channel transfer characteristics: $V_D=0.1$ V, $V_S=0$ V; V_{BG} varies from −6 to 0 V in 1 V increments and (b) back channel transfer characteristics: $V_D=0.1$ V, $V_S=0$ V; V_{FG} varies from −3 to 0 V in 1 V increments.

The bias dependence of RTS due to a trap in the back ONO was measured in the device shown in Fig. 3, with the device biased in strong inversion (beyond threshold voltage) at room temperature, with a drain current of ~10 nA. The bias conditions for the RTS measurements were $V_D=10$ mV, $V_S=0$ V, $V_{\text{FG}}=-2$ V, and V_{BG} was varied between −3.25 and −2.75 V. The linearly extrapolated threshold voltage of the back channel transistor for $V_{\text{FG}}=-2$ V is $V_{\text{BG}}=-3.4$ V [Fig. 3(b)].

RTS was recorded in a time-domain measurement of the source-drain current using a parameter analyzer, with constant voltages applied to front gate, back gate, source, and drain. A maximum of 10 000 points are acquired at a time with a minimum time interval of 80 μs. The sampling interval is adjusted for a particular signal depending on its time scales in order to maximize the number of steps acquired while maintaining adequate time resolution. The two-level signals are analyzed using a search algorithm to locate the switching events and determine the capture times (time spent in the high-current state after a switch-up event) and the emission times (time spent in the low-current state after a switch-down event). The times spent in each state after a random switching event follow a Poisson distribution and the average capture and emission times are given by the means of the respective distributions.[3] The traces used in the RTS analysis have a minimum of approximately 400 switching events per trace.

From the bias dependence of the RTS signal, and with the device biased in strong inversion, the position of the trap in the dielectric can be estimated by[9]

$$\frac{d(\ln \bar{\tau}_c/\bar{\tau}_e)}{dV_G}=-\frac{1}{kT}\frac{d}{dV_G}\left[(E_{\text{Cox}}-E_T)-(E_C-E_F)-\phi_0+q\psi_s+q\frac{x_T}{t}(V_G-V_{\text{FB}}-\psi_s)\right]\approx-\frac{q}{kT}\frac{x_T}{t}$$

where $\bar{\tau}_c$ and $\bar{\tau}_e$ are the average capture and emission times, E_{Cox} is the bottom of the oxide conduction band, E_T is the energy level of the trap, E_C is the bottom of the silicon conduction band, ϕ_0 is the silicon–silicon oxide conduction band offset, ψ_s is the silicon band bending, V_{FB} is the flatband voltage, x_T is the position of the trap in the dielectric relative to the silicon–silicon dioxide interface, and t is the dielectric thickness. This equation follows from the principle of detailed balance (same rate for capture and emission processes) together with the occupation probability of the trap as being given by Boltzmann distribution. The trap occupation probability is therefore a function of the gate voltage through the energy level of the trap relative to the Fermi level. The underlying assumption for the last term approximation is that the silicon surface potential changes slowly with the gate bias compared to the energy level of the trap in the oxide which is true following the onset of strong inversion.[1–3]

Figures 4(a) and 4(b) show the back-gate bias dependence of RTS due to a trap located in the back ONO stack and the ratio of the capture and emission times versus back-gate voltage from which the location of the trap is determined. Using the expression above, this trap is located approximately 1.3 nm away from the silicon–silicon dioxide interface which corresponds to an oxide trap within the tun-

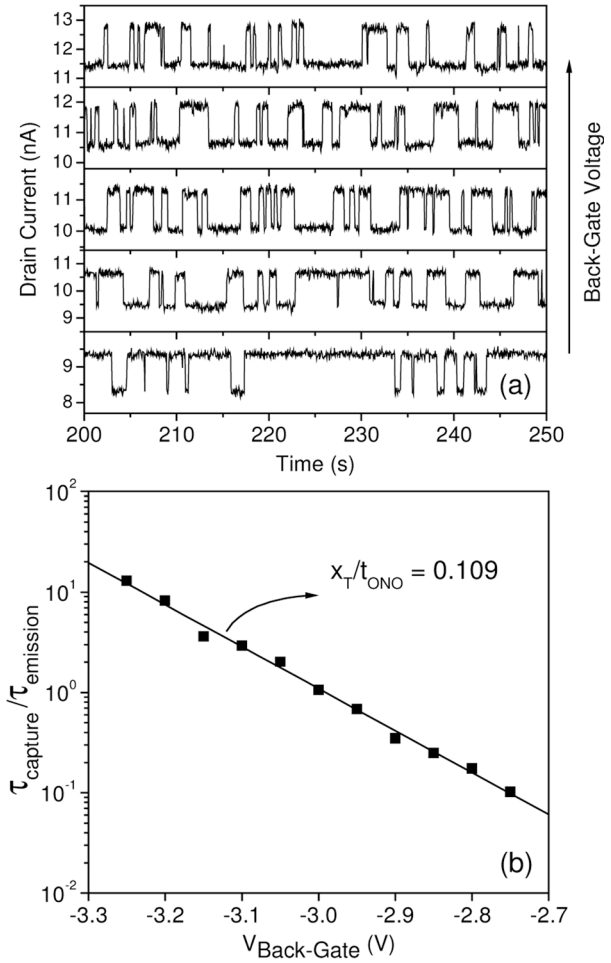

FIG. 4. (a) RTS due to a trap located in the back ONO stack for five different back-gate voltages for the device shown in Fig. 3. $V_{BG}=-3.2$, -3.1, -3.0, -2.9, and -2.8 V. $V_D=10$ mV, $V_S=0$ V and $V_{FG}=-2$ V. $V_{T,BG}=-3.40$ V. (b) Ratio of average capture time and average emission time as a function of the back-gate bias. V_{BG} varies from -3.25 to -2.75 V in 50 mV steps.

neling oxide. These signals have time constants between 200 ms and 5 s.

Prior reports on RTS[1–3,9] in the $Si-SiO_2$ system have shown that traps can be shallow, located at the silicon–silicon oxide interface, or deeper, in the silicon oxide, within a tunneling distance from the silicon interface. Our measurements on multiple interfaces within the same device structure also show shallow and deeper traps and we did not observe traps deeper than ~2 nm.

In summary, we have observed RTS due to traps in the front oxide and in the back ONO stack of back-side trapping memory devices. Bias dependence of RTS due to a back ONO trap shows that the trap is located within the tunneling oxide, at approximately 1.3 nm from the silicon–silicon oxide interface. RTS due to deeper traps, in the silicon nitride or its interface, was not observed. It is important to note, however, that due to the much higher trap density of SiN ($\sim 10^{12}-10^{13}$ cm^{-2}),[7] compared to the $Si-SiO_2$ system ($\sim 10^{10}$ cm^{-2}),[3] the probability of having a two-level RTS signal (due to an individual trap) from a nitride trap is much lower than that from an oxide trap. In a 200 nm × 50 nm device we can expect to have ~1 oxide trap and ~100–1000 nitride traps.

In charge trapping devices with tunneling oxides thinner than ~2 nm, it might be possible to observe RTS due to traps responsible for the memory properties, possibly with distinct characteristics from those in the silicon oxide. However, RTS arises from both a capture and release process, and observation of RTS signals would also indicate a very short storage time in such memory structures.

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