Phase-change oscillations in silicon microwires

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We have observed liquid-solid phase-change oscillations in 2–5.5 μm long silicon wires biased through a load resistor. Molten silicon resistivity is approximately 30 times lower than that of the room temperature solid-state resistivity of the highly doped nanocrystalline-silicon thin film used to fabricate the wires. Wires typically melt with 15–20 V electrical stresses, draining the parasitic capacitance introduced by the experimental setup within 1 μs. The power dissipated in the wire is not sufficient to keep it in molten state after the discharge, leading to repeated melting and resolidification of the wires with 1 MHz, 2–20 mA current oscillations. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3083553]

Relaxation oscillations[1,2] are observed in systems where an element with a resistance switching characteristic,[3,4] such as discharge tubes,[5] tunnel diodes,[6] bistable quantum hall effect devices,[7] or phase-change random access memory (PRAM) devices,[8–10] is connected in parallel with a capacitor and biased through a load resistor.[11] The hysteretic behavior in the resistance switching of these elements[12] allows the capacitor to charge when the device is in high-resistance state and discharge when the device switches to low-resistance state in repeated cycles. We have observed large amplitude oscillations of this nature due to solid-liquid phase changes in silicon (Si) wires.

The wires used in the experiments are fabricated from a thin film of highly doped nanocrystalline Si with room temperature resistivity of 12.0 ± 2.9 mΩ cm (p-type) or 35.6 ± 0.5 mΩ cm (n-type). Si films are deposited in a low pressure chemical vapor deposition system at 560 °C with high-level *in situ* boron doping or at 600 °C with phosphorus doping on Si substrates with thermally grown oxide. Photolithography and reactive ion etching are used to define the wires with widths (W) from 50 to 400 nm and lengths (L) from 0.5 to 5.5 μm. Ti/Ni metal lines and contact pads are formed using photolithography, metal evaporation, and lift-off processes.[13]

The experimental setup consists of a parameter analyzer that controls a pulse generator unit (PGU), a switch box, and an oscilloscope [Fig. 1(b)]. A load resistor (R_L) is connected between the switch box and PGU in order to allow dc I-V measurements on the wire without R_L. Two oscilloscope channels with 1 MΩ ($\|13$ pF) input impedance are used to monitor the supply voltage (V_{pulse}) and the voltage across the wire (V_{wire}). The oscilloscope and parameter analyzer are controlled by a computer. Approximately two meters of coaxial cable with ~100 pF/m of capacitance and ~0.5 μH/m of inductance are used in the setup.

As-fabricated wires are nanocrystalline/amorphous mixed phase with a negative temperature coefficient of resistance (TCR). Contact resistance (R_C) between the probes and Si wire, due to the probes contacting the metal pads, the metal lines, the metal lines contacting Si pads leading to the wire, and the Si pads, is 2.5–5 kΩ. The melting temperature of bulk Si ($T_{melt\ Si}$) is ~1415 °C (Ref. 14) and the resistivity of liquid Si is 7×10^{-5} Ω cm.[14–16] Sufficiently high currents (>20 MA/cm^2) forced through the wires lead to self-heating and melting.[17] The self-heating process in conjunction with the wire's negative TCR results in positive feedback. Wire resistance (R_W) decreases as joule heating increases, causing an increase in dissipated power ($P_{wire} = V_{wire}^2/R_W$) leading to a thermal runaway and melting. R_C is reduced to ~1 kΩ, while the wire is molten. The self-heating process cannot be controlled if a constant voltage pulse is applied directly to the wire since R_C is not sufficient to limit P_{wire}, resulting in melting and breaking of the wire. Figure 2 shows four distinct regions of I-t characteristics during self-heating due to a constant voltage pulse. Region 1 is the transient period corresponding to voltage ramp. In regions 2 and 3 the increase in current can be attributed to thermal carrier generation, annealing of wire defects, dopant activation, and growth of nanocrystal size.[18,19] The increase in current in region 4 is due to melting, and the wire is completely molten when current reaches a plateau. The wire breaks and stops conducting at the end of region 4.

Applying a triangular voltage pulse to the wire is a more controllable method of annealing since P_{wire} is forced to decrease by the ramp down in voltage (Fig. 3). Wires which

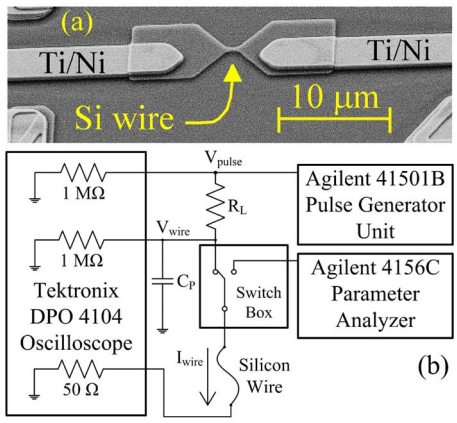

FIG. 1. (Color online) (a) SEM image of a silicon wire with metal contacts and (b) the circuit diagram of the setup used in this experiment. The parasitic capacitances of the load resistor, oscilloscope inputs, and coaxial cables are modeled by the lump capacitor (C_P).

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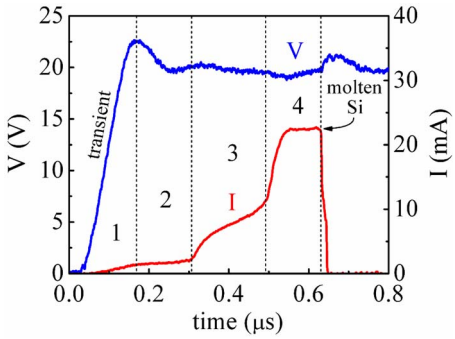

FIG. 2. (Color online) A *p*-type wire with $L=5.5$ μm, $W\sim200$ nm, and thickness ~120 nm is electrically stressed by a constant voltage pulse.

fully melt during high current stresses (critically annealed wires) have positive TCR in lower temperature range and four to ten times lower resistances after stress (R_{WF}) than their as-fabricated resistances (R_{W0}). After a wire is critically annealed, further improvement in its room temperature conductivity saturates. However, if an already critically annealed wire is heated but not melted, wire resistance can be increased up to 50% of R_{W0} (Ref. 18) (an increase two to five times in R_W). This is attributed to concentration of dopants into the grains during resolidification and diffusion of dopants from the grains to the grain boundaries during lower temperature annealing.[18] These annealing processes are used in resistance trimming of heavily doped polycrystalline silicon resistors.[20]

Another controllable method of annealing the wires is to introduce a resistor (R_L) between the wire and PGU. The power delivered to the wire (P_{wire}) is maximized when $R_W=R_L+R_C$ for a given applied voltage. The resistance of the wires in liquid state ($R_{W\ \text{liquid}}$) ranges from ~10 to ~200 Ω. In the case where $R_{WF}<R_L<R_{W0}$, P_{wire} is sufficient for melting an as-fabricated wire. Once the wire reaches liquid state, P_{wire} is drastically reduced and the wire is able to cool down and resolidify. Beyond this point, P_{wire} is not sufficient for melting the wire again with the same bias condition since

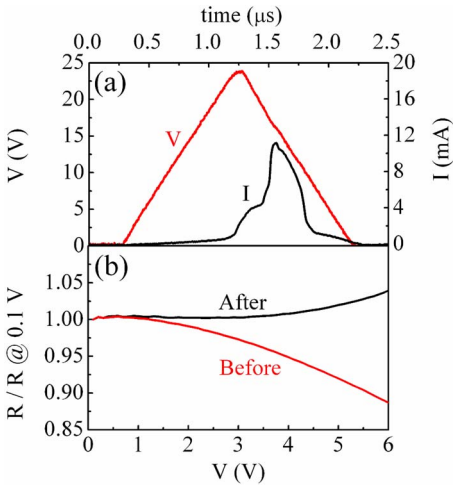

FIG. 3. (Color online) Critical annealing of an *n*-type wire with $L=3.5$ μm, $W\sim130$ nm, thickness ~80 nm. (a) I_{wire} and V_{pulse} vs time during a 24 V triangular pulse. (b) R scaled by R at 0.1 V as a function of voltage for dc sweeps taken before and after the pulse. Resistance at 0.1 V is 51.4 kΩ with negative TCR before the pulse and 4.74 kΩ with positive TCR after the pulse.

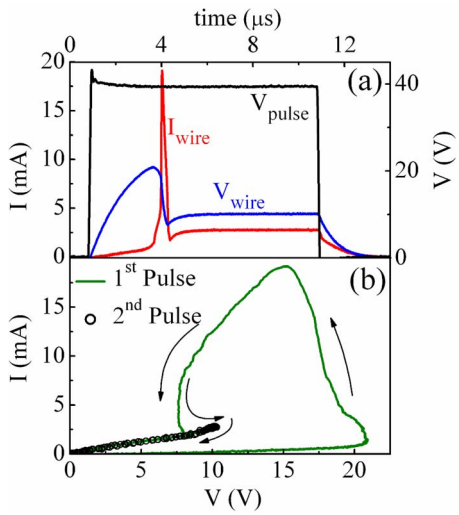

FIG. 4. (Color online) An *n*-type wire with $L=4.0$ μm, $W\sim200$ nm, and thickness ~80 nm is electrically stressed through a load resistor ($R_L=9.92$ kΩ) by a constant voltage pulse. (a) I_{wire}, V_{pulse}, and V_{wire} vs time. (b) I_{wire} vs V_{wire} for the pulse shown in (a) and a following identical pulse. $R_{W0}=36.7$ kΩ, $R_{WF}=3.58$ kΩ.

R_W is significantly reduced. This is seen in Fig. 4(a) as a sharp peak followed by a plateau in *I-t* characteristics, and in Fig. 4(b) as a loop in I_{wire}-V_{wire} characteristics. Applying an identical, consecutive pulse does not result in melting.

However, in the case where $R_{W\ \text{liquid}}<R_L<R_{WF}$, P_{wire} is sufficient for melting both an as-fabricated wire and a critically annealed wire with the same bias condition. Thus, an instability is achieved since P_{wire} is not sufficient to keep the wire in liquid state. This, along with the capacitance from the coaxial cables ($C_P=240$ pF), results in a condition which favors relaxation oscillations for certain bias voltages. The maximum and minimum resistances during the oscillations suggest that a wire can oscillate between completely solid and completely liquid states (Fig. 5), or between different liquid-solid ratios along the length of the wire (Fig. 6). Oscillation amplitude and frequency are determined by R_L, R_W

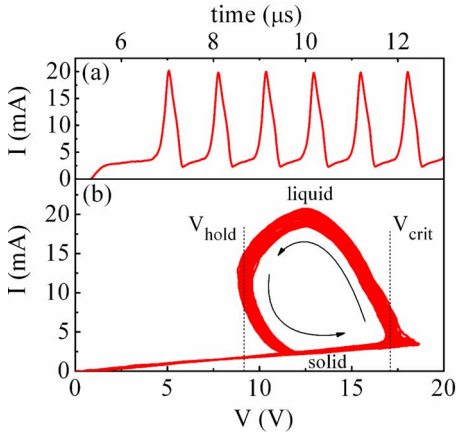

FIG. 5. (Color online) A critically annealed *p*-type wire with $L=2.5$ μm, $W\sim220$ nm, and thickness ~120 nm is electrically stressed through a load resistor ($R_L=1.18$ kΩ) by a 320 μs 23 V rectangular pulse. (a) I_{wire} vs time. (b) A plot of I_{wire} vs V_{wire} suggests that the wire oscillates between completely solid and completely liquid states. Threshold values V_{crit} and V_{hold} (Ref. 21) indicate where the wire is rapidly changing phase. Oscillation frequency=870 kHz.

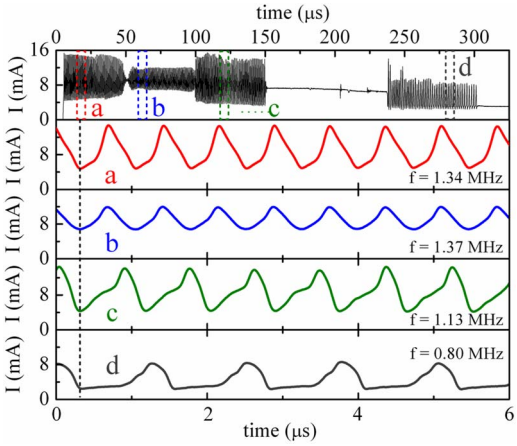

FIG. 6. (Color online) A critically annealed *p*-type wire with $L=2.5$ μm, $W\sim220$ nm, and thickness ~120 nm is stressed through $R_L=1.18$ kΩ by a 320 μs 21 V rectangular pulse. I_{wire} and V_{wire} (not shown) oscillate in four distinct regions (a–d), with constant frequencies within each region (1.34, 1.37, 1.13, and 0.80 MHz). R_W before pulse=2 kΩ, $R_{WF}=5.9$ kΩ.

in solid state ($R_{W\ \text{solid}}$), V_{pulse}, C_P, and the time scale of melting and resolidification.

Every time a wire melts and resolidifies there is a small change in solid-state wire resistance. Each oscillatory period consists of one cycle of melting and resolidification and oscillation amplitude is slightly different in each period. The system is observed to abruptly lose or gain resonance as $R_{W\ \text{solid}}$ changes over a typical time scale of ~50 μs in the case presented in Fig. 6. In this particular case, R_W increases by approximately three times (to about 50% of R_{W0}) and the system oscillates in four distinct regions. Oscillation frequency is in the order of 1 MHz and it is constant within each region.

Relaxation oscillations of this nature have been modeled by Freire *et al.*[21] and Schmidt and Callarotti[1,2] as circuits consisting of a dc voltage supply, load resistor, and a capacitor in parallel with a resistance switching element. These models assume that the resistance switching element remains in high-resistance state ($R_W=R_{W\ \text{solid}}$) until the voltage across the device reaches a threshold value (V_{crit}), where the device instantaneously switches to the low-resistance state ($R_W=R_{W\ \text{liquid}}$). The low-resistance state remains until device voltage drops below a lower threshold value (V_{hold}). Threshold values V_{crit} and V_{hold} are marked in Fig. 5(b). The necessary conditions for oscillation in the Freire[21] model are

$$\frac{V_{\text{pulse}}}{1+(R_L+R_{W\ \text{liquid}})} < V_{\text{hold}} < V_{\text{crit}} < \frac{V_{\text{pulse}}}{1+(R_L+R_{W\ \text{solid}})}. \tag{1}$$

Using this model oscillation period ($T=1/f$) is calculated to be:

$$T=\left(\frac{R_L R_{W\ \text{liquid}} C_P}{R_L+R_{W\ \text{liquid}}}\right)\ln\left[\frac{V_{\text{crit}}(1+R_L/R_{W\ \text{liquid}})-V_{\text{pulse}}}{V_{\text{hold}}(1+R_L/R_{W\ \text{liquid}})-V_{\text{pulse}}}\right] + \left(\frac{R_L R_{W\ \text{solid}} C_P}{R_L+R_{W\ \text{solid}}}\right)\ln\left[\frac{V_{\text{pulse}}-V_{\text{hold}}(1+R_L/R_{W\ \text{solid}})}{V_{\text{pulse}}-V_{\text{crit}}(1+R_L/R_{W\ \text{solid}})}\right]. \tag{2}$$

This model predicts the frequency of the oscillations in Fig. 5 as 830 kHz and in Figs. 6(a) and 6(d) as 1.43 MHz and 845 kHz, respectively, all within 7% of the observed values, capturing the general phenomenon observed in our experiments. A more complete analysis requires modeling of rather complicated changes in the material properties, thermoelectric effects and heat loss from the microwires to the contact pads and to the substrate.

In conclusion, phase-change oscillations in silicon microwires are demonstrated. These relaxation oscillations are similar to what is observed in PRAM.[8–10] The discharge of the parasitic capacitance is due to significant reduction in resistance of the wires as they melt. Parasitic capacitance from coaxial cables limits oscillation frequency to ~1.5 MHz.

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[1] P. E. Schmidt and R. C. Callarotti, J. Appl. Phys. **55**, 3144 (1984).
[2] R. C. Callarotti and P. E. Schmidt, J. Appl. Phys. **55**, 3148 (1984).
[3] L. Chua, IEEE Trans. Circuit Theory **18**, 507 (1971).
[4] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, Nature (London) **453**, 80 (2008).
[5] B. van der Pol and J. van der Mark, Nature (London) **120**, 363 (1927).
[6] E. R. Brown, C. D. Parker, L. J. Mahoney, K. M. Molvar, and J. R. Soderstrom, Appl. Phys. Lett. **58**, 2291 (1991).
[7] G. Nachtwei, N. G. Kalugin, B. E. Sağol, Ch. Stellmach, and G. Hein, Appl. Phys. Lett. **82**, 2068 (2003).
[8] D. Ielmini, D. Mantegazza, and A. L. Lacaita, IEEE Electron Device Lett. **29**, 568 (2008).
[9] I. Karpov, S. Savransky, and V. Karpov, 22nd IEEE Non-Volatile Semiconductor Memory Workshop, 2007 (unpublished), p. 56.
[10] I. V. Karpov, M. Mitra, D. Kau, G. Spadini, Y. A. Kryukov, and V. G. Karpov, Appl. Phys. Lett. **92**, 173501 (2008).
[11] J. W. Nilsson and S. A. Riedel, *Electric Circuits* (Prentice–Hall, Engelwood Cliffs, NJ, 2007), pp. 263–264.
[12] G. D. Fuchs, N. C. Emley, I. N. Krivorotov, P. M. Braganca, E. M. Ryan, S. I. Kiselev, J. C. Sankey, D. C. Ralph, R. A. Buhrman, and J. A. Katine, Appl. Phys. Lett. **85**, 1205 (2004).
[13] The Cornell NanoScale Science and Technology Facility.
[14] H. Sasaki, A. Ikari, K. Terashima, and S. Kimura, Jpn. J. Appl. Phys., Part 1 **34**, 3426 (1995).
[15] H. S. Schnyders and J. B. Van Zytveld, J. Phys.: Condens. Matter **8**, 10875 (1996).
[16] G. Bakan, A. Cywar, C. Boztug, H. Silva, and A. Gokirmak (unpublished).
[17] T. Sameshima, N. Andoh, and H. Takahashi, J. Appl. Phys. **89**, 5362 (2001).
[18] K. Kato, T. Ono, and Y. Amemiya IEEE Trans. Electron Devices **29**, 1156 (1982).
[19] D. W. Feldbaumer and J. A. Babcock, Solid-State Electron. **38**, 1861 (1995).
[20] Y. Amemiya, T. Ono, and K. Kato IEEE Trans. Electron Devices **26**, 1738 (1979).
[21] J. A. Freire, G. A. Dal Moro, R. Toniolo, I. A. Hümmelgen, and C. A. Ferreira, Org. Electron. **7**, 397 (2006).