Melting and crystallization of nanocrystalline silicon microwires through rapid self-heating

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Nanocrystalline silicon microwires are self-heated through single, large amplitude, and microsecond voltage pulses. Scanning electron micrographs show very smooth wire surfaces after the voltage pulse compared to as-fabricated nanocrystalline texture. Voltage-pulse induced self-heating leads to significant conductance improvement, suggesting crystallization of the wires. The minimum resistivity during the pulse is extracted from wires of different dimensions as 75.0 ± 4.6 $\mu\Omega$ cm, matching previously reported values for liquid silicon. Hence, nanocrystalline silicon microwires melt through self-heating during the voltage pulse and resolidify upon termination of the pulse, resulting in very smooth and less-resistive crystalline structures. © *2009 American Institute of Physics.* [DOI: 10.1063/1.3159877]

Amorphous and low-temperature processed polycrystalline silicon films are commonly used in large area electronics applications such as active matrix liquid crystal displays, image sensors, and solar cells due to the advantages of low cost, uniform structure over a large area and low processing temperature.[1,2] However, poor electrical performance of low-temperature processed silicon has impeded integration of high performance circuits with large area electronics on a common platform, such as systems on glass.[3] The demand for higher performance devices on glass and plastics has led to studies on techniques of crystallization of silicon, such as metal induced lateral crystallization (MILC),[4,5] sequential lateral solidification[6,7] and rapid melting and growth from melt of 50–250 μm structures using laser annealing[8] or Joule heating through chromium heaters.[9] These approaches typically result in large-grain polycrystalline Si structures. In this work, melting and resolidification of Si microwires through self-heating using single, microsecond voltage pulses (Fig. 1) is presented.

Silicon wires were fabricated on thin films of nanocrystalline silicon (nc-Si). Both n- and p-type films were deposited on thermally oxidized single crystal silicon substrates in a low pressure chemical vapor deposition system with high-level *in situ* doping ($\sim 5 \times 10^{20}$ cm^{-3}) of phosphorus at 580 °C and boron at 560 °C. Wires are defined using photolithography and reactive ion etching. Wires have design widths (W_d) ranging from 100 to 600 nm with 10 nm increments and lengths (L) from 0.5 to 5.5 μm with 0.5 μm increments. In this paper, results from two different sets of wires are discussed. The first set consists of n-type nc-Si wires, anchored between large-area Si contact pads, suspended by etching the underlying SiO$_2$ using buffered oxide etch [Fig. 2(a)]. The second set consists of p-type nc-Si wires on SiO$_2$, on which 300 nm thick metal contacts (Ti/Ni) were formed using photolithography, metal evaporation and lift-off processes (Fig. 3). Film thicknesses (t) are measured as 80 nm for n-type and 120 nm for p-type films using optical interferometry.

Tungsten needles are used to directly probe the Si contact pads of suspended n-type wires. Figure 1 shows the circuit schematic of the experimental setup. *I-V* characteristics are measured using the parameter analyzer before and after the voltage pulse. Pulse amplitude (V_{pulse}) and current through the wire (I_{wire}) are monitored using the oscilloscope during the pulse. As-fabricated suspended n-type wires are wide and thin with uniform nanocrystalline texture [Fig. 2(a)]. Wires stressed with large amplitude (40 V), short duration (1 μs) voltage pulses acquire smooth surfaces, cylindrical shape, and a lump in the middle [Fig. 2(b)]. Longer duration pulses lead to tapering [Fig. 2(c)], plastic deformation and breaking of the wires [Fig. 2(d)].

The conductance of these wires is enhanced after the voltage pulse unless they break. Figures 2(b) and 2(c) show 2.5 μm long suspended n-type wires of similar widths with total prepulse resistance of 47.8 and 52.4 kΩ, respectively. Total resistance (R_{Si}) consists of the wire (~ 10 kΩ) and contact-pad resistances (~ 40 kΩ). After the pulse, total resistance of the wires in Figs. 2(b) and 2(c) are measured as 19.6 and 20.3 kΩ, respectively. These values are smaller than the prepulse contact-pad resistance. Low postpulse resistance is attributed to conductance enhancement in both the wires and the contact regions, even though the changes in the contact regions are not observable under scanning electron microscope (SEM) [Fig. 2(b)]. The contact-pad resistance
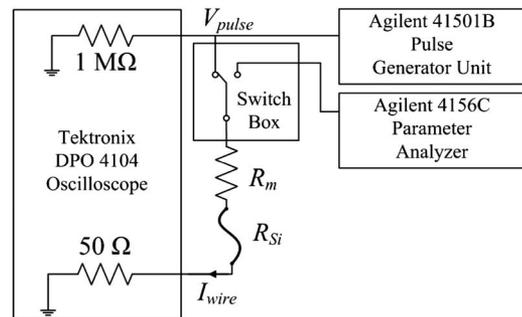

FIG. 1. Schematic of the experimental setup. R_m and R_{Si} are resistances of metal extensions of p-type wires and silicon wires with contact pads, respectively.

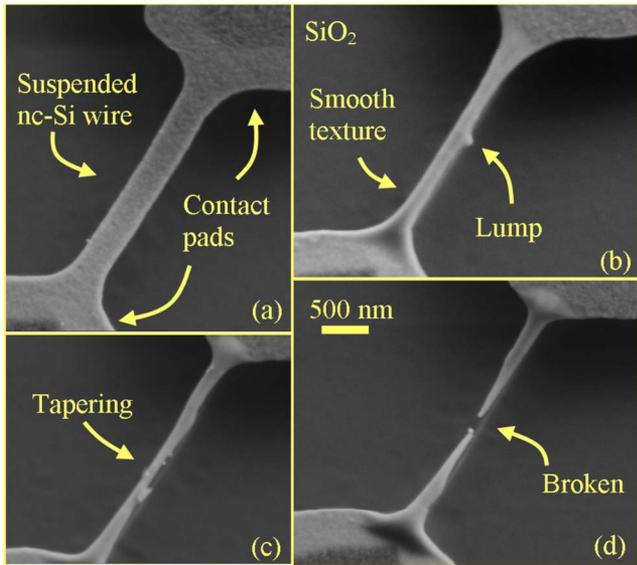a)Electronic mail: gokirmak@engr.uconn.edu.

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FIG. 2. (Color online) SEM images of as-fabricated suspended silicon wire (a) and three other suspended wires after a 40 V pulse of 1 (b), 2 (c), and 5 μs (d) durations. All *n*-type with $L=2.5$ μm.

FIG. 4. (Color online) 20 V, 1 μs voltage pulse (V_{pulse}) and corresponding current (I_{wire}) through a *p*-type wire ($L=5.5$ μm, $W=130$ nm) (a). I_{wire} through 5.5 μm long *p*-type wires with various W during a 20 V, 1 μs pulse (b).

(R_c) in these wires strongly depends on the probe placement on the contact regions, preventing accurate systematic resistance measurements on these suspended wires.

Systematic *I-V* measurements before, during and after the voltage pulse, are performed on *p*-type silicon wires, resting on oxide, with metal (Ti/Ni) contacts (Fig. 3). *I-V* measurements before and after the voltage pulse are performed using low voltage dc sweeps (0–2 V) in order to prevent any resistance changes due to self-heating during the measurement (Fig. 3 inset). Figure 3 shows a 5.5 μm long, 110 nm wide *p*-type wire after a 20 V, 1 μs pulse. I_{wire}-time characteristics of the wire is shown in Fig. 4(b) (W $=110$ nm). Resistivity of the wire decreased by a factor of 4 after the pulse (Fig. 3 inset).

The current (I_{wire}-time) and voltage (V_{pulse}-time) characteristics [Fig. 4(a)] of *p*-type wires during single, 1 μs voltage pulses, as recorded by the oscilloscope, show significant nonlinear changes in the current level during the pulse.[10] Region (i) is the initial transient period. The increase in current in region (ii) is expected due to the negative temperature
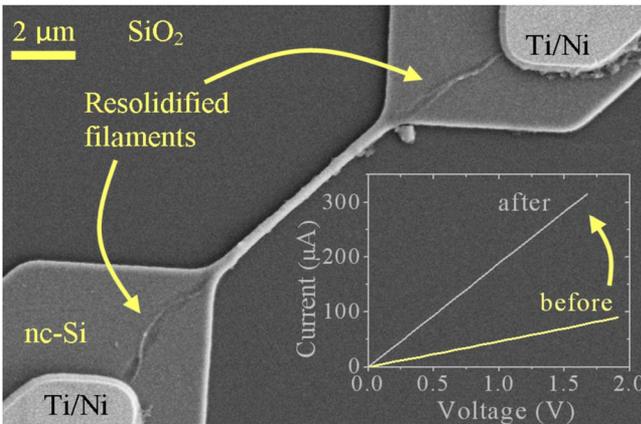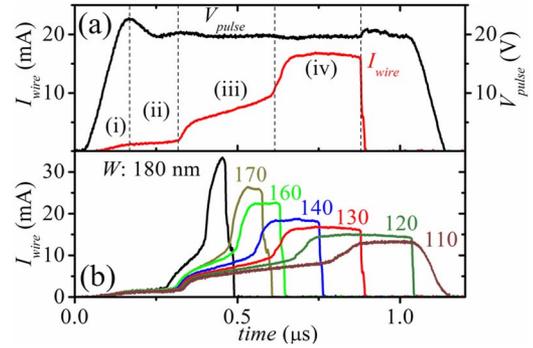
coefficient of resistivity of the as-fabricated material (nc-Si). However, the stepwise and significant changes in current in regions (iii) and (iv), and the observed plateau in region (iv) were not expected. Total resistance (V_{pulse}/I_{wire}) corresponding to the maximum current in region (iv) of Fig. 4(a) is extracted as 1.18 kΩ, whereas the metal line resistance (R_m) for the wire and probes is 840 Ω. Hence the silicon resistance (R_{Si}), including Si contact pad (R_c) and wire resistances, is only 340 Ω during the pulse (1.6% of its initial value).

R_{Si} in region (iv) [Fig. 4(b)] is extracted for wires of various dimensions, accounting for R_m. If the Si wires are assumed to be linear resistors with uniform cross sections along the wire, R_{Si} can be written as

$$R_{Si} = R_c + \frac{\rho}{Wt}L, \tag{1}$$

where R_c is the silicon contact-pad resistance and ρ is the resistivity of Si wires. Effective wire widths (W) deviate from the design widths (W_d) by ΔW ($\sim$250 nm) due to the lithography process. ΔW, hence W, are extracted from systematic resistance measurements on the wires prior to the voltage pulse. Slopes of R_{Si} versus L lines ($\alpha = \rho/Wt$), hence ρ, are obtained from linear regression as seen in Fig. 5. Figure 6 shows ρ obtained from two test sites for various W with estimated errors. The weighted average of ρ is calculated as 75.0 ± 4.6 $\mu\Omega$ cm, without accounting for 5% volume contraction of wires in liquid phase.[11] The errors in ρ (Fig. 6) are due to the errors in film thickness measurements and regres-

FIG. 3. (Color online) SEM image of a *p*-type wire ($L=5.5$ μm, $W=110$ nm) after a 20 V, 1 μs pulse. *I-V* characteristics of the wire before and after the pulse (inset).
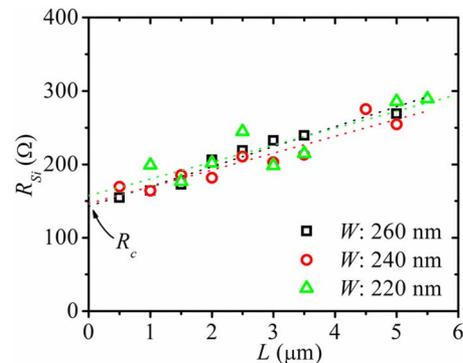

FIG. 5. (Color online) Minimum wire resistance (R_{Si}) during the pulse vs wire length (L) for W from 220 to 260 nm.
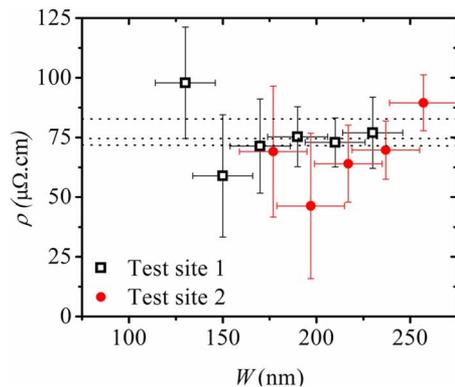
FIG. 6. (Color online) Extracted wire resistivity (ρ) for various W. Dotted lines indicate previously reported liquid silicon resistivity values of 83 $\mu\Omega$ cm (Ref. 11), 75.2 $\mu\Omega$ cm (Ref. 12), and 72 $\mu\Omega$ cm (Ref. 13).

sion errors in α and ΔW. Dashed lines in Fig. 6 show previously reported liquid silicon resistivity values of 83 $\mu\Omega$ cm by Glazov *et al.*,[11] 75.2 $\pm$ 0.6 $\mu\Omega$ cm by Schnyders and Van Zytveld[12] and 72 $\mu\Omega$ cm by Sasaki *et al.*,[13] extracted using bulk silicon with large-scale, high-temperature setups. Close agreement between extracted ρ and the liquid silicon resistivity values indicates that the wires melt due to the applied voltage pulse [Fig. 4-region (iv)]. Additionally, small R_c values (Fig. 5) of the wires during the pulse suggest that the silicon contact pads are also molten during region (iv) of the voltage pulse. Observation of resolidified filaments between the metal contacts and the wire as seen in Fig. 3 supports this argument. Hence, the changes in current in region (iii) and region (iv) are attributed to melting of the wire and filament formations, respectively, resulting in a complete molten silicon path between metal contacts. The wires are expected to melt prior to filament formation due to the thermal boundary conditions. Furthermore, in wires where the applied voltage pulse does not lead to the last step in I_{wire}-time characteristics [region (iv)], there is no evidence of filamentation under SEM. The stability in current in region (iv) once a liquid path is formed between the metal contacts is due to the relative insensitivity of liquid silicon resistivity to temperature.[11] This enables extraction of liquid silicon resistivity using this approach.

MILC studies on amorphous silicon wires show that polycrystalline grains grow longer for narrower wires and tend to form single crystal domains along wires with widths less than 250 nm.[5,14] Hence, solidification of the suspended wires upon termination of voltage pulse [Fig. 2(b)] is expected to yield two continuous grains with low defect density if the wires are narrower than the thermodynamically favored grain size. Strong thermal gradient along the suspended wires, due to low heat loss to the substrate, would suppress nucleation and consequently grain boundaries within these

wires. As the two solid fronts meet in the middle, some portion of the molten silicon cannot fit between resolidified regions due to the higher density of liquid silicon.[11] Excess silicon is ejected and forms a lump upon resolidification [Fig. 2(b)].

In summary, SEM images show very smooth wire surfaces after the wires are self-heated through high amplitude, short-duration voltage pulses, compared to their as-fabricated nanocrystalline texture. Current through the wires shows nonlinear changes during the pulse. Minimum resistivity of the wires, calculated from *I-V* characteristics during the voltage pulse, matches with previously reported liquid silicon resistivity values. The postpulse resistivity of the wires is typically 4 times smaller than their as-fabricated values. These findings are evidence of melting of the wires by self-heating during the voltage pulse, and crystallization of the wires upon termination of the pulse. Resolidification of the wires starts from the two ends of the wire and the resolidified regions meet in the middle. Two crystalline domains are expected to form in presence of a strong lateral thermal gradient if the wire is narrower than the thermodynamically favored grain size. These results indicate that crystallization of patterned micro/nanostructures through voltage pulse induced self-heating can be a viable crystallization approach, compatible with a variety of substrates. Additionally, the presented approach used for calculation of resistivity during short-duration voltage pulses is a submicrometer scale, low-cost alternative for extraction of molten materials resistivities.

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