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Measurements of Liquid Silicon Resistivity on Silicon Microwires

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ABSTRACT

Nanocrystalline silicon microwires are self-heated through microsecond voltage pulses. Nonlinear changes in current level are observed during the voltage pulse, which end with melting of the microwires. Liquid silicon resistivity is extracted as 65.9 ± 6.1 μΩ.cm from the minimum resistance of the wire during the voltage pulse. The extracted resistivity is in good agreement with previously reported values.

INTRODUCTION

Interest in achieving high mobility thin-film transistors (TFTs)[1] for large area electronics[2] has motivated studies on crystallization of amorphous and polycrystalline silicon for several decades. Most of the crystallization techniques such as sequential lateral solidification using an excimer laser[3], rapid melting and growth from melt of large patterned-films using YAG laser[4] or Joule heating through chromium heaters[5], or melting and crystallization of silicon microwires through rapid self-heating[6, 7] involve growth from the melt[8] which has increased the interest in the properties of molten silicon. Liquid silicon properties such as electrical resistivity, thermopower, density and viscosity have been reported since 1960s. Electrical resistivity measurements have been performed using the electrodeless method in a rotating magnetic field[9] or four-point probe method using a macroscopic volume of molten silicon[10, 11]. Material selection for container and electrical contacts is very important for accuracy and reliability of the measurements in these setups due to the high melting temperature of silicon (1420 C)[9]. In this work, liquid silicon resistivity is obtained by performing wafer-level measurements on nanocrystalline silicon (nc-Si) microwires with various dimensions through microsecond voltage pulse induced self-heating.

Fabrication

Microwires are patterned on a nc-Si film which is deposited in a low pressure chemical vapor deposition system at 560 C with high-level in-situ boron doping (~5×10^{20} cm^{-3})[12] on a thermally oxidized Si substrate. Si wires have design widths (W_D) ranging from 300 to 500 nm with 10 nm increments and lengths (L) from 0.5 to 5.5 μm with 0.5 μm increments. Wires are formed using photolithography and reactive ion etching. Wire lengths (L) match well with the design dimensions. Film thickness (t) at the center and the edge of the wafer is measured as 123 and 130 nm, respectively, using optical interferometry and as 128 ± 9 nm on a Si contact pad using atomic force microscopy (AFM). AFM result for t is used to calculate Si resistivity in both solid and liquid phases. Ti/Ni (250/60 nm) electrodes are formed by photolithography, metal

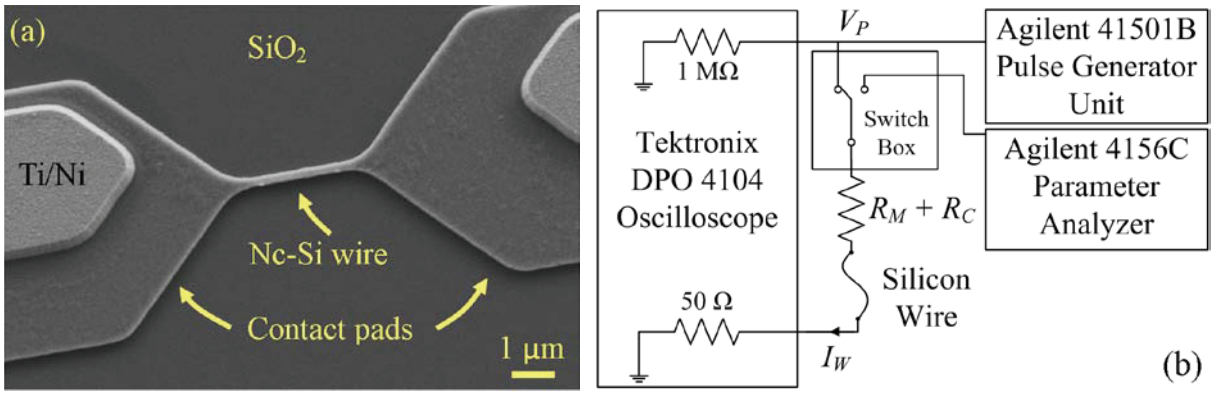

Figure 1. (a) An as-fabricated, 3 μm long, p-type, nc-Si wire. (b) Schematic of the experimental setup. R_M and R_C are resistance of metal extensions and silicon contact pads, respectively. Applied-voltage amplitude (V_P) and current through (I_W) the wire are captured by the oscilloscope.

evaporation and lift-off processes to make reliable ohmic contacts between electrical probes and the Si wires (Figure 1a).

EXPERIMENT

Figure 1b shows the experimental setup. I-V characteristics of the wires are measured by the parameter analyzer before and after the voltage pulse. Total resistance extracted from the I-V characteristics includes the resistance of the metal (Ti/Ni) extensions (R_M) and silicon resistance (R_{Si}), where R_{Si} is sum of silicon contact pad (R_C) and wire resistance. Although R_M is different for each silicon wire, it is calculated accurately using known metal extension lengths. The Si wires are treated as linear resistors with uniform cross section along the wire length. Thus, R_{Si} is written as:

$$R_{Si} = R_C + \frac{\rho}{Wt} L \qquad (1)$$

where ρ is the wire resistivity and W is the effective wire width. R_{Si} measured on wide wires is used to extract the unknown parameters, since R_{Si} versus L is not fairly linear for narrow wires ($W_D < 400$ nm). R_C is found as the y-intercept of linear fit of R_{Si} versus L (Figure 2a). Slope of R_{Si} versus L lines (α), W, and t are the key parameters to extract the wire resistivity. W is, however, unknown and typically ~ 220 - 300 nm (ΔW) narrower than W_D. Although ΔW changes with exposure dose and thickness of Si, SiO_2 and photoresist layers, linear fit of $1/\alpha$ versus W_D reveals ΔW at the x-intercept (Figure 2b). Hence, resistivity of the wires is calculated as $\rho = \alpha W t$. The resistivity of the wires is calculated as 8.1 ± 0.5 mΩ.cm at room temperature, accounting the errors associated with linear regression and film thickness measurement. The four point-probe measurement on the nc-Si film gives a resistivity of 11.2 ± 0.8 mΩ.cm at room temperature.

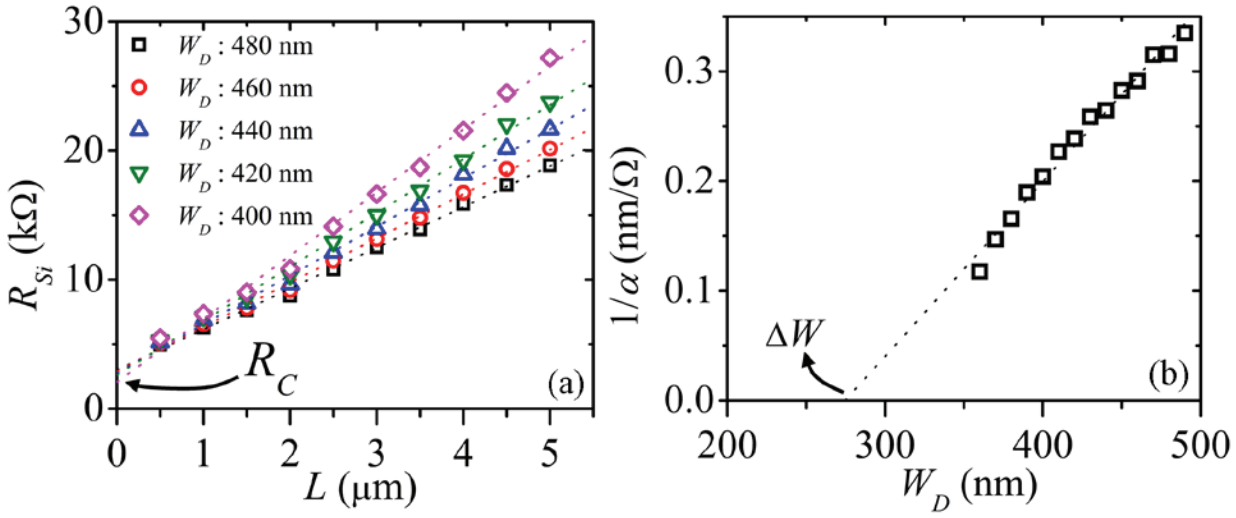

Figure 2. (a) Silicon resistance (R_{Si}), including the silicon contact pad (R_C) and as-fabricated wire resistance, as a function of wire length (L). (b) Reciprocal of R_{Si} versus L line slope ($1/\alpha$) versus design width (W_D). Average deviation (ΔW) of effective width (W) from design width (W_D) is 275 nm for this test site.

I-V characteristics of the wires during the pulse are also extracted from current (I_W) – time and voltage (V_P) – time characteristics captured by the oscilloscope. Nonlinear changes in current level are observed (Figure 3a) when single, high amplitude (~20 V), microsecond voltage pulses are applied across the wires (Figure 3b - top). Figure 3b shows an applied voltage-pulse amplitude (V_P) and resulting current (I_W) through a p-type wire (L = 5 μm, W = 155 nm). Although V_P is almost constant during the pulse, I_W increases drastically through a series of transitions. In the initial transient period (Figure 3b - region (i)), I_W ramps from zero to a low current level (~1.5 mA) as V_P increases from 0 to 16.4 V. I_W increases with a slow rate in region (ii). This small increase in I_W suggests that as-fabricated wires have negative temperature

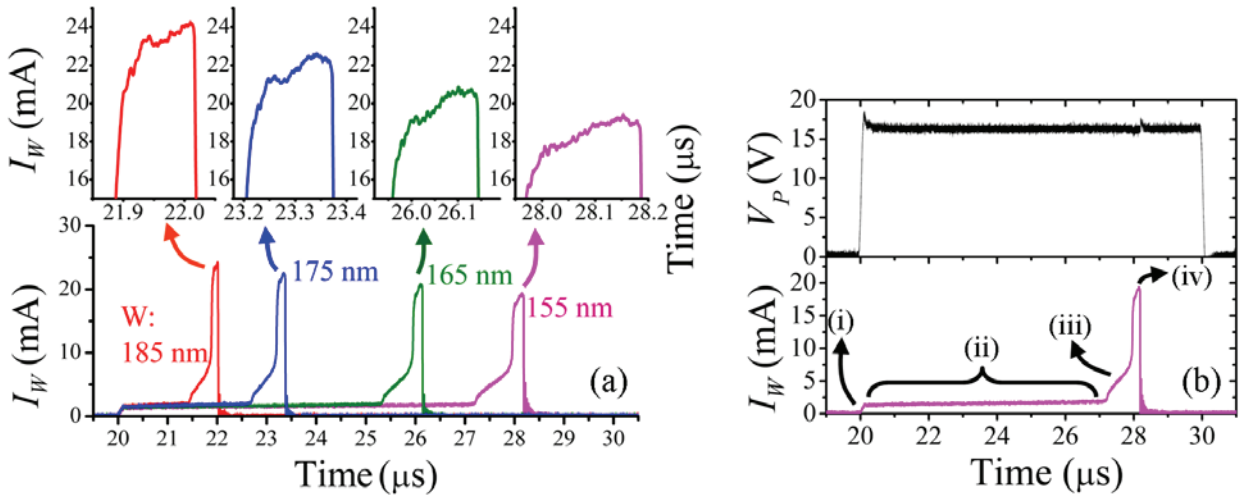

Figure 3. (a) Current (I_W) – time characteristics of four wires with indicated widths (L = 5 μm). Peak of each I_W curve is seen on top. (b) Applied voltage pulse (V_P) on a p-type wire (L = 5 μm, W = 155 nm) and corresponding current (I_W), showing four distinct regions in I_W – time characteristics.

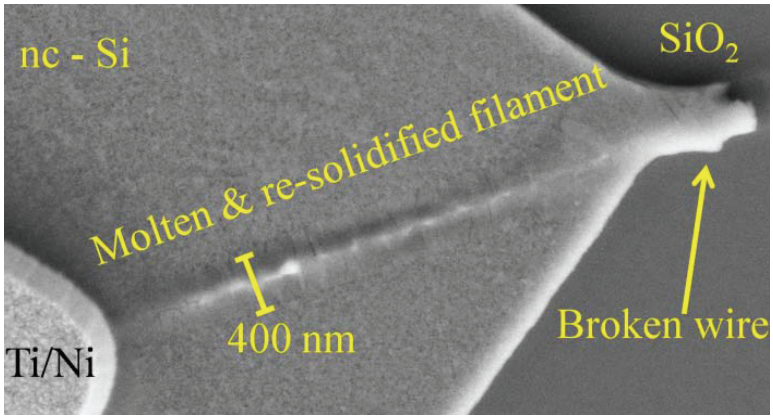

Figure 4. Resolidified filament on silicon contact pad of a wire, broken after 14 V, 1 μs voltage pulse.

coefficient of resistivity. First abrupt increase in I_W level (Figure 3b - region (iii)) is attributed to melting of the wire. Second, and final, increase (Figure 3b - region (iv)) indicates melting of narrow current paths (filaments) on the silicon contact pads (Figure 4). Therefore, a continuous liquid silicon path forms between the two metal (Ti/Ni) contacts in region (iv) (Figure 3-top). Melting order of silicon between the metal contacts is inferred from I_W –time characteristics with SEM analysis of the wires that do not show the second abrupt increase in I_W (region (iv)).

Wires eventually break after I_W reaches region (iv) of I_W –time characteristics, unless the voltage pulse is terminated. The duration between entire melting and breakdown strongly depends on wire dimensions (Figure 3a) and the amplitude of the applied voltage pulse, V_P. Increase in I_W in the region (iv) is attributed to widening of filaments on Si contact pads, resulting in less resistive paths between the wire and the metal contacts. Liquid silicon resistance (R_{Si}) values for wires of different dimensions are extracted from the minimum total resistance ($R_M + R_{Si}$) during the pulse.

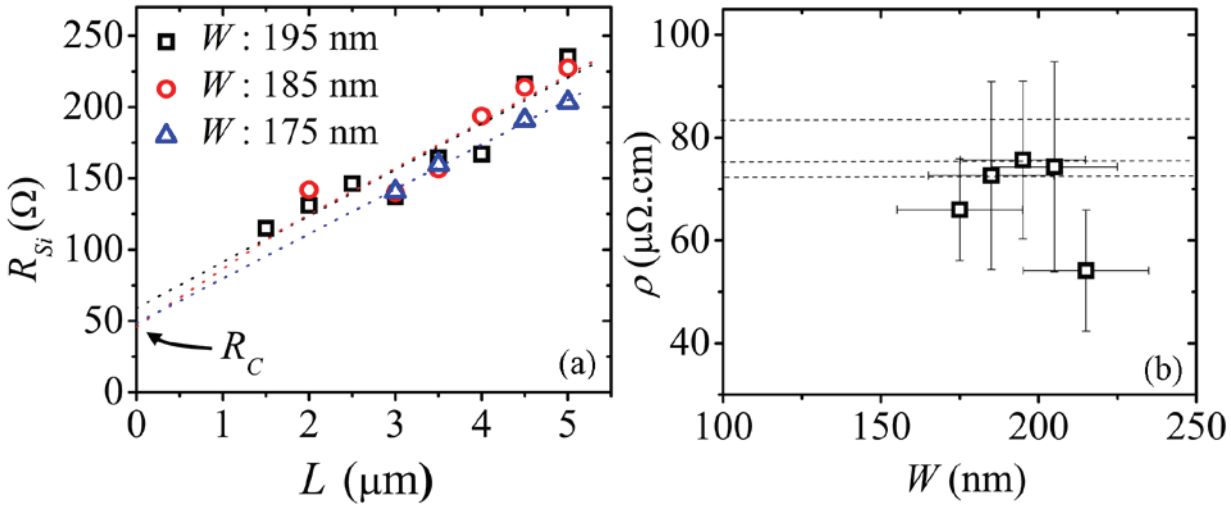

Figure 5. (a) Liquid silicon resistance (R_{Si}) as a function of wire length (L) for three W arrays (175 - 195 nm). Molten filament resistance (R_C) is found as ~ 50 Ω. (b) Liquid silicon resistivity (ρ) versus W. Dashed lines indicate previously reported values, 83 μΩ.cm by Glazov et al. (Ref. 9), 75.2 ± 0.6 μΩ.cm by Schnyders et al. (Ref. 11) and 72 μΩ.cm by Sasaki et al (Ref 10).

Table 1. Reported experimental liquid-silicon resistivity values and respective methods.

ρ (μΩ.cm)	*Reference*	Method
65.9 ± 6.1	*This work*	*Wafer level*
83	Glazov et al. (Ref. 9)	Electrodeless (in a rotating magnetic field)
75.2 ± 0.6	Schnyders et al. (Ref. 11)	4- point probe
72	Sasaki et al. (Ref. 10)	4- point probe

The statistical method used to extract resistivity of as-fabricated wires is also performed for the wires in liquid phase. Liquid silicon resistance, R_{Si}, versus L plots (Figure 5a) are sufficient to extract liquid silicon resistivity, ρ, since cross section, Wt, of the wires are already known from previous as-fabricated wire resistivity analysis. Figure 5a shows R_{Si} as a function of L for three W arrays, revealing the resistance of molten filament, R_C, as ~50 Ω at the y-intercept. Liquid silicon resistivity, ρ, as a function of W with estimated errors is shown in Figure 5b.

Weighted average of ρ is calculated as 65.9 ± 6.1 μΩ.cm, accounting for the 5 % volume contraction of wires in liquid phase[9]. The errors in ρ (Figure 5b) are due to uncertainty in film thickness measurements and regression errors in α and ΔW. Previously reported values, using melt of large silicon volumes, are given in Table 1 and indicated as dashed lines in Figure 5b.

CONCLUSION

A sub-micrometer scale, wafer-level technique to determine the liquid silicon resistivity is presented. nc-Si wires with various widths and lengths are stressed and melted by large amplitude, microsecond voltage pulses. Ease of fabrication, local heating and melting, using conventional probe station and standard semiconductor electrical characterization instruments as the experimental setup are the advantages of the presented technique over other liquid material resistivity measurement methods[9-11]. Error in the liquid silicon resistivity can be reduced by increasing the variety of the wire dimensions and decreasing the error in the film thickness measurement. Obtained liquid silicon resistivity value is in close agreement with previously reported experimental results (Table 1). This micrometer scale, wafer-level technique is a convenient way of measuring liquid silicon resistivity and it can be used to measure the liquid phase resistivity of other materials.

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