A Silicon Nitride Based Shallow Trench Isolation with Side-Gate for CMOS Integration with MEMS Components for System-On-Chip Applications

Ali Gokirmak and Sandip Tiwari
School of Electrical and Computer Engineering, Cornell University,
Ithaca NY 14853, U.S.A.

ABSTRACT

We have developed a hydrofluoric acid (HF) resistant, composite shallow trench isolation (STI) process for MOSFETs utilizing silicon nitride as isolation material for on-chip integration of micro-electro-mechanical (MEMS) resonators and CMOS devices. Peripheral leakage currents in silicon nitride isolated MOSFETs are suppressed by employing an independently controlled polysilicon side-gate, surrounding the active area of the devices. Electrostatic control of the threshold voltage at the device periphery alleviates the need for edge implants, resulting in increased thermal budget. Compatibility with HF release processes and high temperature anneal cycles allows integration of MEMS components in close proximity to CMOS devices for system-on-chip applications. nMOSFET devices fabricated using this composite STI process show excellent device characteristics.

INTRODUCTION

High quality factor micro-electro-mechanical resonators have been demonstrated as good alternatives to conventional RF filters [1]. Significant power reduction can be achieved if these MEMS elements can be integrated on chip with the CMOS circuitry for system-on-chip applications (e.g. mobile communications). Integration of MEMS resonators and passive components on the same chip can also lead to significant reduction in packaging and assembly cost. Two challenges in the integration of most MEMS components with CMOS fabrication process are; compatibility with HF based sacrificial oxide removal process and high temperature deposition and anneal cycles.

Processes used for the fabrication of suspended polysilicon structures, like micro-mechanical resonators, extensive rely on HF removal of sacrificial SiO_2 in order to release polysilicon structures [2,3]. The requirement of HF release process makes it very hard to integrate CMOS circuits utilizing SiO_2 STI in close proximity to MEMS structures. One possible approach to overcome this problem is to use HF resistant isolation material for shallow trench isolation of the CMOS devices.

Silicon nitride (Si_3N_4) is a CMOS compatible, HF resistant dielectric material which can be used for STI process [3]. Mechanical stress, electrical leakage, high interface defect density at

Si-Si_3N_4 interface and high concentration of fixed charges in the as deposited Si_3N_4 films are challenges to be addressed in order to use a Si_3N_4 based STI process for CMOS devices.

In this work we demonstrate excellent nMOSFET device characteristics down to 125nm length scale, utilizing a silicon nitride based STI process with polysilicon side-gates, compatible with HF release and high temperature anneal steps.

DISCUSSION

High density stochiometric silicon nitride films with good electrical characteristics can be deposited using low pressure chemical vapor deposition (LPCVD). However, as deposited stochiometric silicon nitride films have high tensile stress, high density of positive trapped charges, and lead to high density of Si-Si_3N_4 interface defects when deposited on bare Si surface.

The stress level in these films can be reduced by increasing the silicon content in the film, which in return lead to increased electrical leakage. One possible solution to this problem is to use a combination of a thin stochiometric silicon nitride layer and a thicker silicon rich low-stress silicon nitride layer, as it is used in this work.

Fixed positive charges in the Si_3N_4 film and at the active-STI interface for nMOSFET devices lead to reduced threshold voltage on the device edges [4] hence lead to higher leakage currents and degrade subthreshold characteristics. Defects at the active-STI interface lead to increased generation current resulting in increased drain to substrate leakage [5]. It is possible to increase the threshold voltage at the device edges by introducing higher concentration of dopant atoms at the interface. This approach is limited by the diffusion of the dopants during the possible high temperature cycles required by the MEMS processes. The degradation in device characteristics due to diffusion of the dopants, introduced at the device periphery, is more significant for nMOSFET devices as boron is used as the primary p-type dopant in silicon devices. Electrostatic control of the threshold voltage at the device edges via an independently controlled side-gate, surrounding the active area of the device is a viable method to suppress the edge-related leakage currents in order to achieve the required low power CMOS performance with low leakage currents [6,7] (Fig.1).

DEVICE DESIGN and FABRICATION

In this work we used 350 nm of n+ in-situ-doped polysilicon as the side-gate metal as a part of a composite STI structure. In fully integrated circuits groups of devices or modules can share the same side-gate and a thinner layer of polysilicon can be used in order to minimize the area penalty. The composite STI structure is

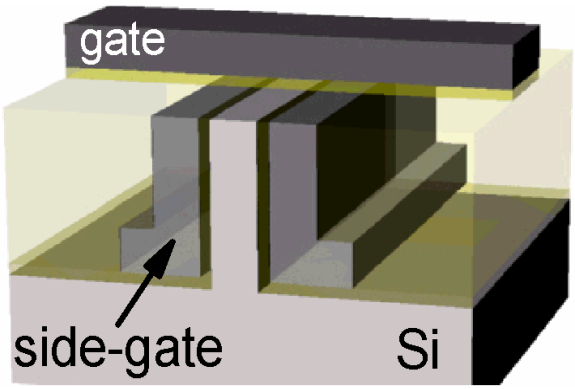

Figure 1. 3D device schematics

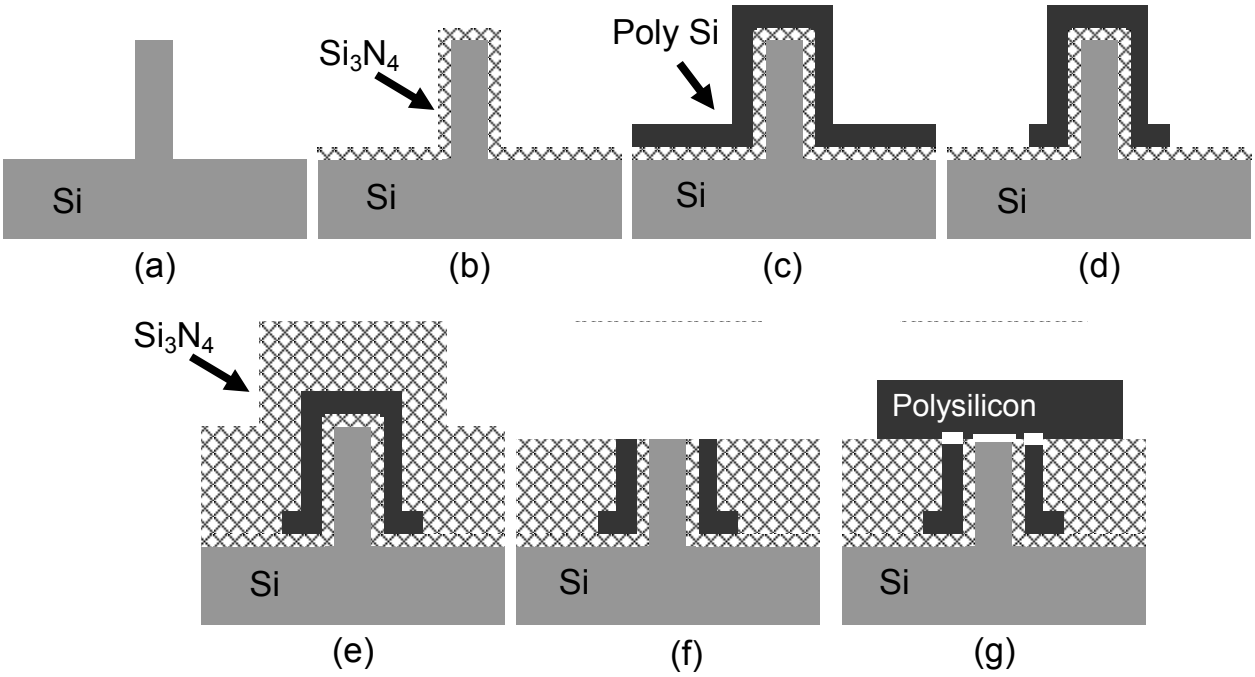

Figure 2. Composite STI fabrication steps

formed by slight alterations to the conventional STI process. The active areas of the devices are defined by photolithography and etched down using anisotropic reactive ion etch (RIE) (Fig.2a). After cleaning the sidewalls a thin layer (19nm) of Si_3N_4 and a thicker layer (350nm) of n+ in-situ-doped polysilicon is deposited (Fig.2b-c). Polysilicon film, which will be used as the side-gate, is patterned around the active areas with an extension, leading to a contact area, using optical lithography and RIE (Fig.2d). A thin layer of Si_3N_4 and a thicker layer of low stress silicon nitride films are deposited (Fig.2e). The STI process is finalized by a chemical mechanical polishing (CMP) step, polishing off the top part of the silicon active areas (Fig.2f).

The polishing rate of single crystal silicon in the CMP process is slower compared to polysilicon and SiO_2 but it is faster than silicon nitride. This results in height variations on the top surfaces up to 10's of nm. The height of different films can be adjusted slightly by thermal oxidation, HF wet etch and short CMP steps to achieve the desired topography. After this step thin gate oxide is grown both on Si active areas and the surrounding polysilicon side-gate, another layer of polysilicon is deposited as top-gate and patterned (Fig.2g). After thin

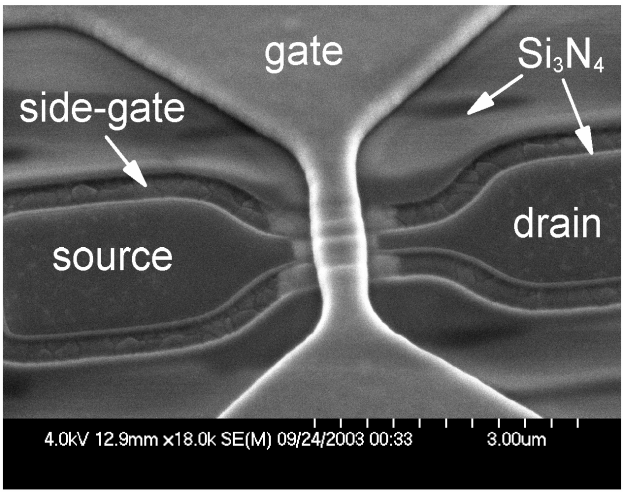

Figure 3. SEM image before passivation.

side-wall formation high dose shallow source/drain As implants are done (Fig.3), followed by passivation. Vias for contacts are opened and metal contacts are deposited. Sidewalls and passivation layers can be made using SiO_2, Si_3N_4 or any other compatible material depending on the requirements of the MEMS processing steps need for the integration at this point. In this case we used thermally grown SiO_2 as side-wall spacers and plasma enhanced chemical vapor deposition (PECVD) SiO_2 as passivation material.

ELECTRICAL CHARACTERISTICS

DC current-voltage characteristics of abrupt n^+-p junctions formed at the source/drain & substrate interfaces are measured as a function of side-gate bias (V_{side}) (Fig.4). Drain to substrate reverse-bias leakage current decreases as a function of V_{side} down to about -1.5V as the interface is accumulated with holes [5]. After this point the leakage current starts to increase again which can be explained by increased band to band tunneling known as gate induced drain leakage (GIDL) [8]. No change in the on current of these diodes is observed as V_{side} is varied.

Drain to source leakage currents are also significantly suppressed by applying a negative V_{side} as the Si-STI interfaces are turned off (Fig.5). Other device characteristics such as subthreshold slope (SS), drain induced barrier lowering (DIBL), on current (I_{on}), transconductance (g_m) and response of the threshold voltage (V_t) to V_{side} vary significantly depending on the topography of the channel surface. Slight changes in the CMP and post CMP processes prior to gate formation can lead to devices which have a planar surface profile or a profile resembling a tri-gate structure (Fig.6) where the top-gate wraps over the channel on the

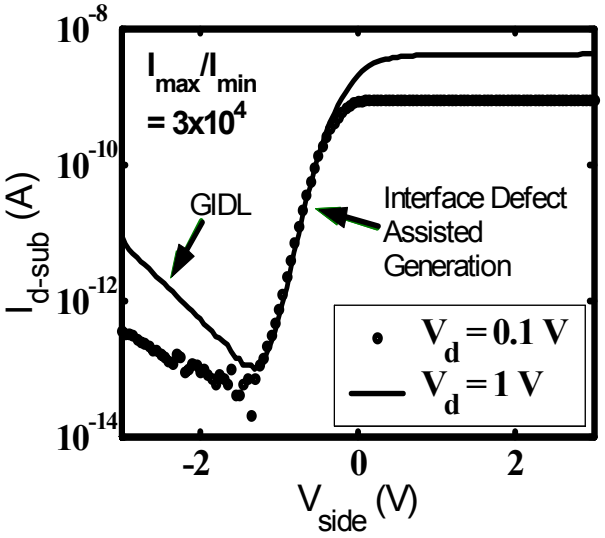

Figure 4. Reverse-bias leakage current of a drain to substrate diode as a function of V_{side}. Area ~ 6 μm², perimeter ~ 18 μm.

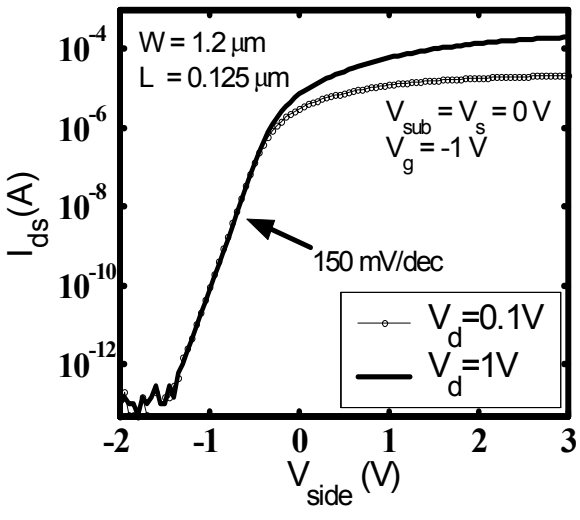

Figure 5. Drain to source leakage current as a function of V_{side}.

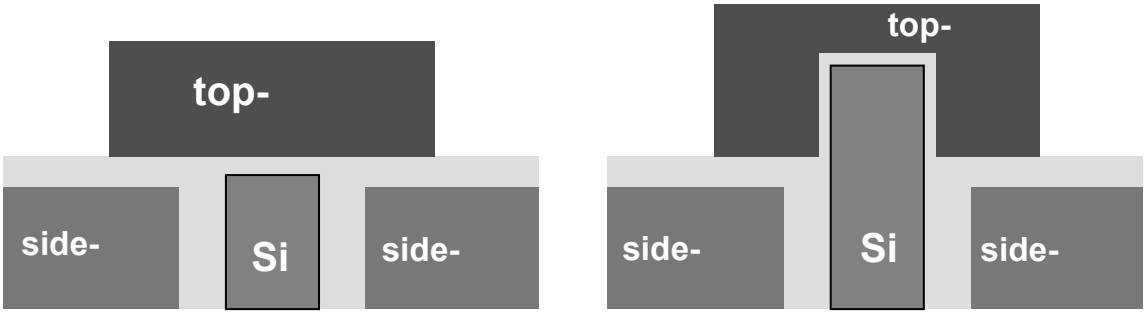

Figure 6. Planar (left) and tri-gate (right) bulk side-gated device geometries.

top [9,10]. In the planar geometry the channel potential is controlled both by the V_{side} and the V_g, leading to a device with V_t tuning capability by adjusting the V_{side}, but results in poorer subthreshold slope [7]. In the tri-gate case, the top-gate control on the device channel is increased and the effect of the V_{side} on the V_t of the device is reduced. Moderately recessed side-gate structures show small V_t change and improvement in subthreshold slope as a function of increased negative V_{side}. In the extreme recessed side-gate case the V_{side} does not have any effect on V_t or the subthreshold slope of the device, however, increased I_{on}, g_m reduced DIBL and subthreshold slope are observed.

The nMOSFETs demonstrated here are fabricated without using any halo implants or silicidation. The extreme tri-gate devices, with no V_t response to V_{side}, fabricated at 0.25µm gate length with 1.2µm effective width with 4.3nm gate oxide show; DIBL= 13.65mV/V, SS= 69mV/dec., I_{on}/I_{off} exceeding $1.1x10^{10}$ for V_d=1V. The drive current (I_d) of these devices go up to 0.77mA/µm for V_g=V_d=3V. Measured parameters for 125nm effective gate length devices are DIBL=70mV/V, SS= 81mV/dec, $I_{on}/I_{off} > 1.1x10^{10}$ for V_d=1V and I_d= 0.83 mA/µm for V_g=V_d=3V (Fig.7). High-field mobility calculated for these devices do not show degradation

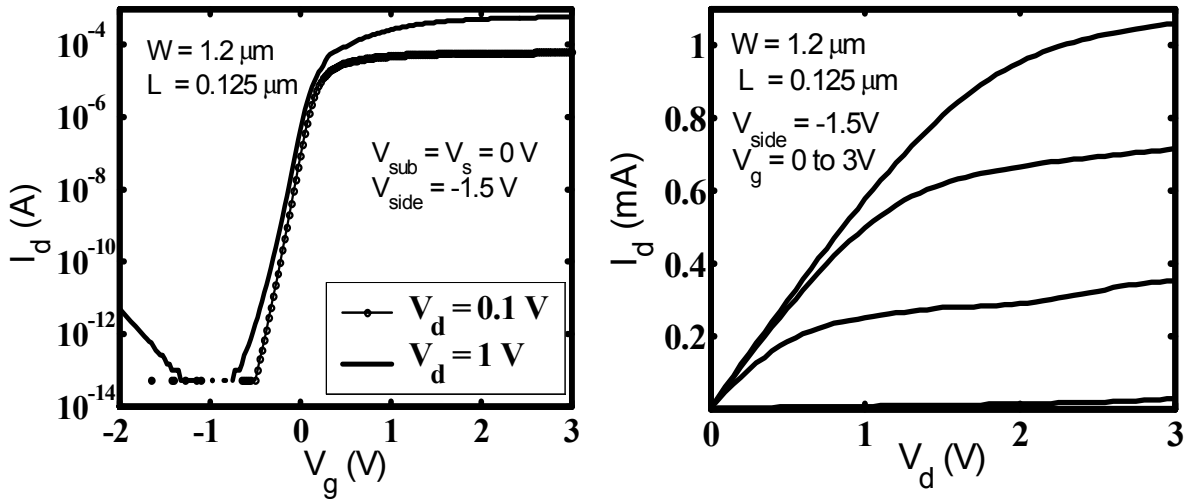

Figure 7. Drain current as a function of Vg (left) and drain current as a function of V_d (right) characteristics for a side-gated bulk tri-gate structure.

compared to standard silicon devices.

CONCLUSION

We have demonstrated a HF resistant composite STI process using silicon nitride and a polysilicon surround side-gate. nMOSFET devices fabricated using this process show excellent DC device characteristics. Electrostatic suppression of the edge related leakage currents using the side-gate eliminates the need for threshold voltage adjustment implants on the device edges, hence, leading to higher compatibility with high temperature anneal and deposition steps after the formation of the CMOS structures. HF resistant STI together with increased thermal budget allows a higher degree of freedom for integration with MEMS components on the same chip in close proximity to CMOS devices for system-on-chip applications.

REFERENCES:

1. S.-S. Li; Y.-W. Lin; Y. Xie; Z. Ren, C.T.-C Nguyen, 17th IEEE International Conference on Micro Electro Mechanical Systems, 821–824 (2004).
2. J. Buhler, F.-P. Steiner, H. Baltes, J. Micromech. Microeng, **7**, R1-R13 (1997).
3. R. T. Howe, J. Vac. Sci. Technol. B **6** (6) 1809-1813 (1988).
4. P. Sallagoity, M. Ada-Hanifi, M. Paoli, M. Haond, **43** (11) 1900-1906 (1996).
5. G. Verzellesi, G. F.D. Betta, L. Bosisio, M. Boscardin, G. U. Pignatel, G. Soncini, IEEE Trans. Elec. Dev., **46** (4) 817-820 (1999).
6. P. VanDerVoorn, D. Gan, J. P. Krusius, IEEE Trans. Elec. Dev, **47** (6), 1175-1182, (2000).
7. A. Gokirmak, S. Tiwari, IEE Electronics Letters (2004) (Submitted)
8. L. Huang, P. T. Lai, J. P. Xu, Y. C. Cheng, Microelectronics Reliablity, **38**, 1425-1431 (1998)
9. D. Hisamoto, W.-C. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asano, T. J. King, J. Bokor, C. Hu, IEDM Tech. Dig., 1032-1034 (1998)
10. B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, and R. Chau, , IEEE Elec. Dev. Let., **24** (4) (2003)