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Pentagate Approach to Reduce the Line Edge Roughness Effects in Bulk Si Tri-gate Transistors

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ABSTRACT

Accumulated body [1] approach to mitigate the effects of line edge roughness on bulk silicon finFETs and tri-gate FETs is analyzed through 3D TCAD simulations. A side-gate surrounding the body portion of the FET is used to accumulate the body with majority carriers. This approach is predicted to reduce device-to-device variability due to line edge roughness by stronger accumulation of the body in the wider sections of the channel and confinement of the channel away from the edges.

INTRODUCTION

Line edge roughness (LER) has been a limiting factor in gate scaling of silicon MOSFETs [2]. Recently, however, with the introduction of lithographically defined thin body devices such as FinFET and Tri-gate FETs, LER started to affect the active region of MOSFETs as well [3, 4]. Grazing incidence ion beams [5] and high temperature hydrogen annealing [6] have been proposed to reduce LER, which was shown to result in significant silicon diffusion with LER reduction from ~ 2.8 nm to 0.8 nm. In this work, instead of focusing on reduction of LER itself, we study an electrostatic method to reduce the effects of LER, through the use of a guard-ring gate surrounding the body of the FET.

THEORY

The pentagate approach

We have previously shown that gating the body of a Si MOSFET with a side-gate biased such as to accumulate the Si body (Figure 1) reduces off-state leakage currents by countering the effect of positive fixed charges and passivating defects at the at the Si body / dielectric interface and enables significant threshold voltage tuning [1].

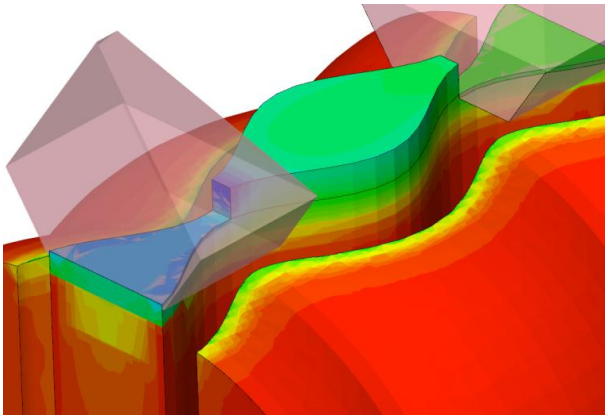

Figure 1. 3D electron density graph of a pFET with applied side-gate bias. Red indicates a density of 1.1×10^{21} cm^{-3}.

In a case where the body edge is severely non-uniform due to LER, the side-gate follows the edges of the body. The normal electric field converges on convexities while diverging on concavities on the side surfaces, resulting in stronger accumulation of majority carriers in convex portions, electrostatically smoothing the channel pathway for the minority charge carriers (Figure 2).

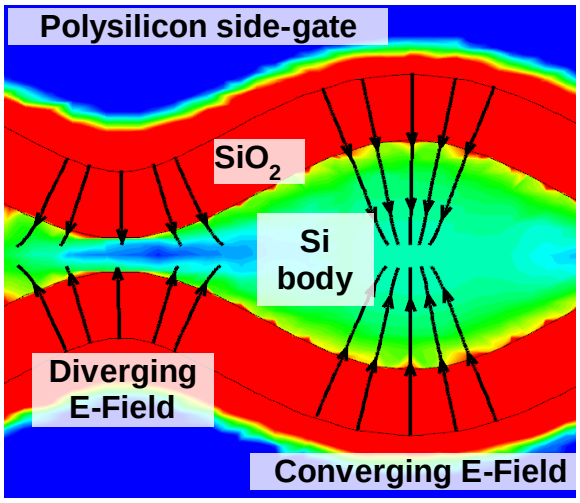

Figure 2. Cross-section of a simulated silicon body surrounded by a polysilicon side-gate. Diverging and converging electric fields (arrows) follow LER and electric field intensity (color) is higher on wider regions of the body.

Simulation

We have simulated 3-D tri-gate n- and p-FET structures with LER to study the effect of the side-gate on the device characteristics, using Synopsys Sentaurus TCAD tools [7]. The simulation tools were used to create various sinusoidal LER cases with varying amplitudes imposed on a nominal width (shown in Table I). An idealized fabrication process was simulated, after which the electrical characteristics of the resulting devices were analyzed.

Table I. LER amplitude and location combinations tested. n-type and p-type FETs with side-gates as well as control devices without side-gates were simulated for these 9 LER cases.

		LER Location			
		Narrow Center	Wide Center	Narrow Source	Narrow Drain
LER Amplitude	0 nm				
	1 nm				
	3 nm				

53 nm tall fins with LER were formed on a low-doped bulk silicon substrate. The top 3 nm portion of the fin is strongly coupled to the tungsten metal gate (top-gate). 5 nm HfO_2 was used as the top-gate dielectric. The bottom 50 nm were surrounded by the side-gate through a 2 nm thermally grown silicon dioxide side-gate dielectric (Figure 3). Control devices were also simulated in which the remaining 50 nm are surrounded by silicon dioxide (STI, shallow trench isolation). Source and drain regions were formed by faceted epitaxial growth. The gate length and nominal width for all simulated cases are 16 nm and 8 nm respectively.

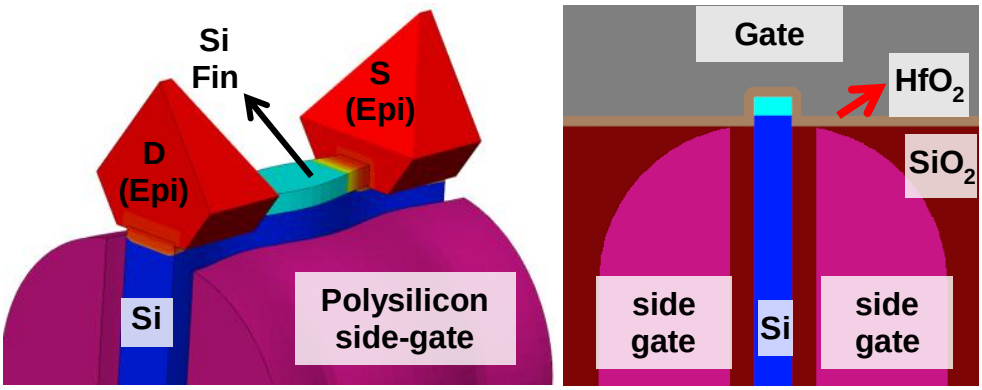

Figure 3. Si body with imposed sinusoidal LER of 1 nm amplitude. Gate and dielectrics are not shown (left). Vertical cross-section image at the FET channel center for a side-gated device. Top 3nm (cyan) is covered by the gate (right).

RESULTS

Transfer characteristics of the side-gated devices (in accumulation) show lower off-state current as well as improved short channel effects such as drain induced barrier lowering (DIBL), as previously reported for side-gated planar FETs [1] (Figure 4).

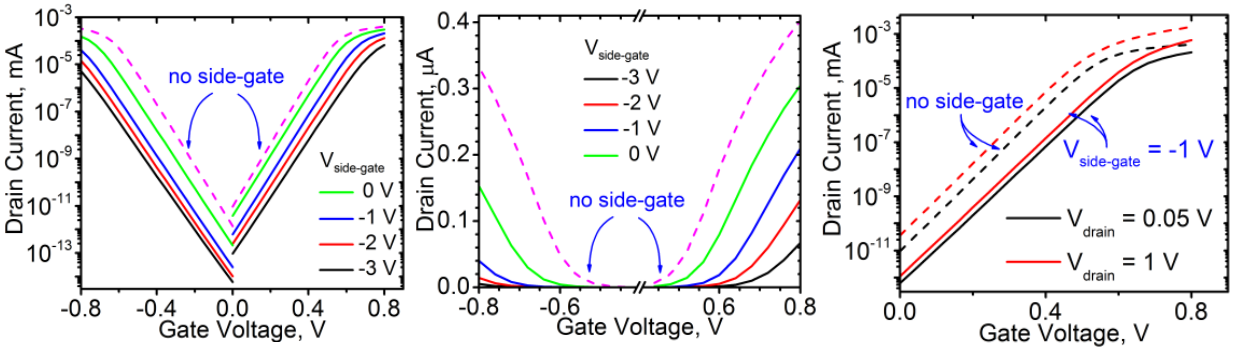

Figure 4. Transfer characteristics in log (left) and in linear scale (middle) for an nFET and a pFET with wide-center LER of 3 nm amplitude. Dashed lines are for control devices with no side-gate. Drain bias is 50 mV. High and low drain bias transfer curves (right) for the nFET device with no side-gate and side-gate bias of -1 V, showing reduced DIBL.

In applications where drain and source can be used interchangeably, asymmetric channel geometries due to LER can display different electrical characteristics and the use of a side-gate to accumulate the body may reduce this variation. Figure 5 illustrates this point by comparing a 'narrow source' and a 'narrow channel' pMOSFET, with and without a side-gate. A visible difference between the two transfer characteristics is observed in the no side-gate devices. With a side-gate bias of -1 V the two transfer characteristics converge, showing the effect of the side-gate in reducing the effect of the LER induced asymmetry.

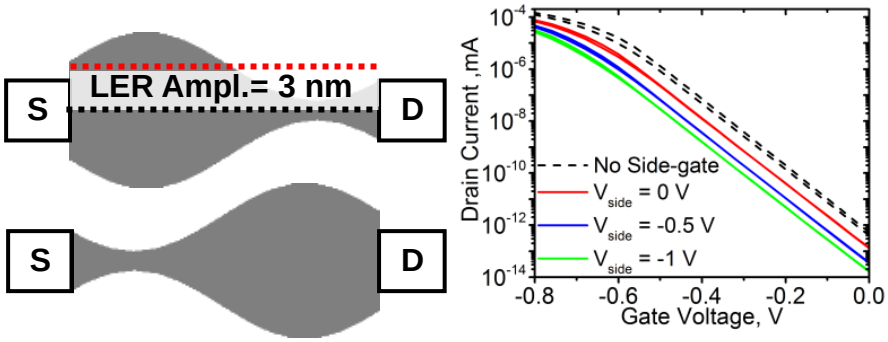

Figure 5. Transfer characteristics for a 'narrow source' and 'narrow drain' pFET cases with no side-gate, and with side gate bias of 0, -0.5 and -1 V. With the side-gate bias, the 'narrow source' and 'narrow drain' characteristics overlap showing effective reduction of the LER induced variability.

In addition to the enhancement of individual devices, accumulation of the device body is expected to improve device-to-device variations among a variety of LER conditions. While the improvements are visible on devices with enlarged source or drain end (Figure 5), not all cases show an improvement. In essence, LER variations impact the device-to-device variations the most if the line width variations are at the source end, where the source-barrier controls the injections of the charges into the channel. The variations in the rest of the channel are rather benign as long as the average width remains approximately the same and impact of the side-gate is also not noticeable.

In summary, body accumulation using a side-gate can be used as an electrostatic approach to reduce LER effects on devices where source and drain are desired to be used interchangeably. Also, low off-state current provides this technique some applications in low-

power electronics. On the other hand, in this approach, an area penalty is inevitable due to the additional side-gate contact. The side-gate approach may be a viable way to reduce LER induced variability especially at the source-end. This approach is expected to be even more effective in planar devices due to increased coupling of side-gate to the MOSFET channel, versus fin- or tri-gate devices in which the geometry limits the proximity of the side-gate.

ACKNOWLEDGMENTS

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REFERENCES

[1] A. Gokirmak and S. Tiwari, "Accumulated body ultranarrow channel silicon transistor with extreme threshold voltage tunability " *Appl. Phys. Lett.*, vol. 91, pp. 243504, 2007.

[2] A. Asenov, S. Kaya and A. R. Brown, "Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness," *Electron Devices, IEEE Transactions on*, vol. 50, pp. 1254-1260, 2003.

[3] E. Baravelli, A. Dixit, R. Rooyackers, M. Jurczak, N. Speciale and K. De Meyer, "Impact of Line-Edge Roughness on FinFET Matching Performance," *Electron Devices, IEEE Transactions on*, vol. 54, pp. 2466-2474, 2007.

[4] M. L. Fan, Y. S. Wu, V. P. Hu, C. Y. Hsieh, P. Su and C. T. Chuang, "Comparison of 4T and 6T FinFET SRAM Cells for Subthreshold Operation Considering Variability—A Model-Based Approach," *Electron Devices, IEEE Transactions on*, vol. 58, pp. 609-616, 2011.

[5] C. R. M. Struck, M. J. Neumann, R. Raju, R. L. Bristol and D. N. Ruzic, "Grazing incidence ion beams for reducing LER," in 2008, pp. 71402P.

[6] S. Bangsaruntip, G. M. Cohen, A. Majumdar, Y. Zhang, S. U. Engelmann, N. Fuller, L. M. Gignac, S. Mittal, J. S. Newbury, M. Guillorn, T. Barwicz, L. Sekaric, M. M. Frank and J. W. Sleight, "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1-4.

[7] Synopsys Inc., "Sentaurus TCAD User Manual," 2011.